# Reliability Assessment of the Integrity of Aluminum Interconnect for a FDSOI Process using Finite Element Techniques

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## Introduction

Silicon-on-insulator (SOI) technology uses a thin layer of silicon (tens of nanometers) isolated from a silicon substrate by a relatively thick (hundreds of nanometers) layer of silicon oxide. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances, and thus, eliminates the possibility of latch-up failures. SOI technology simplifies manufacturing process by eliminating well and field implantation steps and allows fabrication of smaller, denser, and faster microcircuits, with reduced interconnect cross-talk. These features make SOI technology particularly attractive in emerging system-on-chip microcircuits, micro-electromechanical systems (MEMS), and integrated optics applications. Dielectric isolation in SOI also helps in decoupling the analog and digital components in mixed-signal microcircuits by reducing the substrate cross-talk.

The primary motivation for developing SOI technologies was the need for radiation-hardened ICs as an alternative to expensive silicon on sapphire (SOS) technology that uses a thin film of silicon grown on an insulating $Al_2O_2$ substrate. A potentially high radiation tolerance of the SOI devices makes them very attractive for space applications. Analysis of the present state of the art of SOI technology and reliability has shown that SOI technology has relatively matured over last several years and is considered good candidates for aerospace applications. A number of companies are currently testing and evaluating custom designed SOI devices for high volume, commercial manufacturing product lines.

A major objective of this task was to gain some experience with fully depleted SOI technology and the reliability assessment of ultra-fine conductors used in Massachusetts Institute of Technology, Lincoln Laboratory (MIT/LL) FDSOI process.

## Reliability Characterization of MIT/LL FDSOI Process Summary

The previous report for SOI technologies device level characterization task that was titled, "Reliability Evaluation of Fully Depleted SOI (FDSOI) Technology for Space Applications (Part I)" was posted on the NEPP web site. This report provided a general overview of SOI technology including materials, process, reliability issues, and MIT/LL FDSOI processes and associated reliability test structures. The hot carrier degradation effects in the MIL/LL FDSOI FETs at $V_g = V_d/2$ conditions, which are known to maximize the interface trap generation have been investigated at JPL.

Another report on MIT/LL FDSOI process titled, "Reliability Evaluation of MIT/LL FDSOI 0.25 μm Process for Space Applications (Part II)" was also posted on the NEPP web site. This report addressed characterization of the N- and P-channel transistors, including scaling effects and estimation of the reproducibility of the front- and back-channel parameters. The transistor measurements included threshold voltage, subthreshold slope, mobility of charge carriers, gate leakage currents, and investigation of the edge effects.

For the (Part II) evaluation, four process monitor dice were received from MIT/LL, containing NMOS/PMOS transistors of various sizes. The front- and back-channel N- and P-type transistors manufactured in MIT/LL 0.25 μm SOIFD technology were fully characterized using three process monitor dice with 40 transistors in each die (the gate length varied from 0.2 μm to 8 μm and the gate width varied from 0.5 μm to 100 μm). The test results are summarized below.

- The variations in the threshold voltage and the subthreshold slope did not exceed 12% and 20 % (respectively for $V_{th}$ and S). Characteristics of the front channels in NMOS FETs were much less reproducible than for the PMOS transistors.
- Both N- and P-channel transistors exhibited the short channel effect. The absolute values of the threshold voltage decreased significantly below 0.5 μm. The effect was most pronounced for PMOS transistors. A decrease in the gate width, also resulted in a decrease of the absolute value of the threshold voltage.
- The subthreshold slope also showed a strong gate-length dependence, significantly increasing in the submicrometer region (more than twice for the back channel, and approximately 15% - 25% for the front channel transistors).
- The mobility of the charge carriers virtually did not change with the gate length for the front-channel NMOS transistors and increased for the PMOS transistors when the gate length decreased below 0.5 μm.
- Electrical measurements showed that the gate length deviations did not exceed 2% of their drawn value.
- The specific resistance of the gate oxide was approximately $10^{15}$ Ohm*m and the gate leakage current was in the femto-ampere range.
- The parasitic side-wall transistor at the gate edge resulted in some deviations of the transconductance characteristics for the NMOS transistors with the gate width below 2 μm. However, no excessive leakage currents in the OFF condition of the transistors, or any other significant anomalies were observed.

## Reliability Assessment of the Integrity of Aluminum Interconnect for a FDSOI Process using Finite Element Analysis Techniques

The reliability assessment on the integrity of aluminum interconnect was performed on the MIT/LL FDSOI test structure element supplied by JPL. The reliability assessment included thermal stress analysis and heat transfer analysis using finite element techniques. A detailed test report is included in the Appendix A.

## Acknowledgements

This work was supported by NASA Electronics Parts and Packaging (NEPP) Program funded by NASA HQ and performed under the task titled, "Reliability Evaluation of Ultra-Fine Conductors and Contacts in Advanced, Ultra-Low Power Processes". Acknowledgements are due to Udo Lieneweg at JPL for supplying the test structures elements for FEA work support.

# APPENDIX A

# Reliability Assessment of the Integrity of Aluminum Interconnect for a FDSOI Process using Finite Element Techniques

## Part I – Thermal Stress Analysis
## Part II – Heat Transfer Analysis

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**Reliability Assessment of the Integrity of Aluminum Interconnect for a FDSOI Process using Finite Element Techniques**

**Part I – Thermal Stress Analysis**

## 1-1. Introduction

With the ever decreasing dimensions in modern microelectronic devices, thermal-mechanical reliability of the tiny metallic interconnection lines has become a very important factor for the overall performance and reliability of the microelectronic systems. Among many issues, the stress-induced voiding in the interconnection lines remains to be the one of the major concerns in the microelectronic device industry. The purpose of this study is to numerically analyze the thermal-mechanical behavior of the Al interconnection line using FEA methodologies. The results are expected to provide useful guidance for the further study of the reliability issues relating to the Al metallization.

This study is divided into two parts:

**Part I** Thermally-induced stress analysis for the Al interconnection line under the following 2 conditions:

(i) the device undergoing from 400 °C (the dielectric deposition temperature, zero-stress state) to 20 °C (the room temperature);

(ii) the device undergoing from 20 °C to 400 °C—assumption is made that the stress relaxation process is sufficiently long and the room temperature is the zero-stress state.

**Part II** Steady-state conductive and naturally convective heat transfer analysis for the Poly-Silicon layer under the following conditions:

(i) the conduction is the only mode of heat transfer;

(ii) natural convection and conduction are combined in the mode of heat transfer;

In the first part, the driving force for the thermal stress is the change of the ambient temperature ($\Delta T = \pm 380$ °C). However, the temperature variation in part (2) is caused by the electric current flowing through the polysilicon stripe (0.1 A in the second part). The Part II results are presented and discussed in the later sections of this report.

## 2-1. The Configuration to be Analyzed

Fig. 1-1 shows the 2-D cross-section of the device to be analyzed. Due to the tiny dimensions of the Al line, the width of the device can be numerically treated as infinitely long. Fig. 2-1 is the corresponding FEA model for this section, and a total of 1115 shell elements are used for the construction of the model. The width of the model is taken as 48 times the width of the Al line, thus satisfying the infinite approximation for the displacement boundary conditions on both left and right far edges. The bottom of the section is completely restrained. Fig. 3-1 shows the finer elements used for the Al line and its vicinity.

## 3-1. Material Properties

Table 1-1 lists the material properties used for the analysis:

Table 1-1

| | E [GPa] | $\nu$ | $\alpha$ [1/°C] | Yield Strength [MPa] |
|---|---|---|---|---|
| Al | $69.7 - 3.68\times10^{-2}$ T | 0.33 | $23.3\times10^{-6} + 1.66\times10^{-8}$ T | 207 – 0.349 T |
| $SiO_2$ | 71.4 | 0.16 | $0.51\times10^{-6} + 5.4\times10^{-10}$ T | -- |
| Poly-Si | 160 | 0.28 | $2.6\times10^{-6}$ | -- |

Note: The units for T is °C.

The use of the temperature-dependent property data is necessary due to the large temperature variations ($\Delta T = \pm 380$ °C) encountered in the numerical simulation. This will improve the accuracy of the results.

## 4-1. Analytical Results and Discussions

Using the ABAQUS nonlinear procedures for the stress analysis, we obtained the stress distributions in the cross-section of the Al line. Fig. 4-1 shows the overall Von Mises stress distributions at 400 °C throughout the whole FEA model under the temperature change from 20 °C to 400 °C. One can easily observe that the highest stress concentration is around the Al line. To further examine the details of the stress in the Al, Figs. 5-1 and 6-1 reveal the Von Mises stress distributions on the cross-section of the Al line. It is seen that the highest stress is at the four corners of the Al line, the magnitude

being 706.4 MPa. The lowest stress is at the center of the Al line and the magnitude is around 401.5 MPa.

Figs. 7-1, 8-1 and 9-1 show the similar stress distributions under the temperature change from 400 °C to 20 °C. The stress behavior around the Al line is very similar, but the highest Von Mises stress for this scenario is 644.2 MPa. The Al line center stress is about 351.0 MPa.

Using Al's yield strength value listed in Table 1-1, we can find that the Al yields at 200.02 MPa at 20 °C, and 67.4 MPa at 400 °C. This indicates that, in both cases, the Al line has yielded well before reaching the final temperature conditions (400 °C in the first case, and 20 °C in the second). To obtain an idea as to at what temperature the Al yielded, we used the temperature change for the first case (from 20 °C to 400 °C) to perform an iterative analysis to find that temperature. Based on the yield strength data in Table 1-1, we found that the Al line starts to yield at 138 °C and the onset yield stress at this point is 158 MPa.

Obviously, a further investigation is required to characterize the fatigue behavior of the Al line. The stress analysis itself is not sufficient to reveal the cycle-to-failure fatigue life of the Al line. Instead, we must perform nonlinear stress analysis using the constitutive model of plasticity for the Al to obtain the plastic strain range under the given thermal conditions and to estimate the low-cycle fatigue life of the Al metallization using the metal fatigue theory.

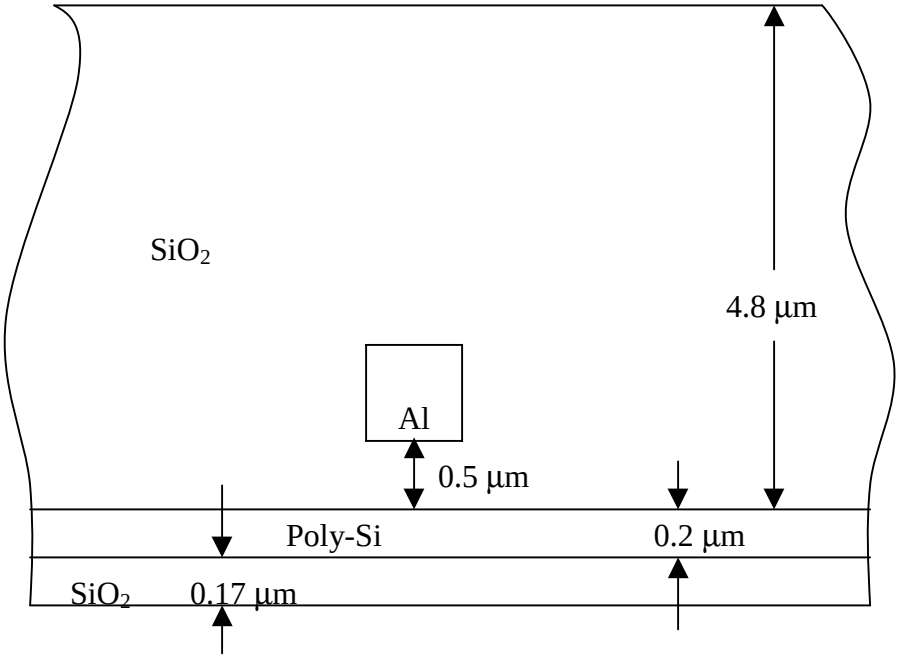


Fig. 1-1 Cross-section of the device (Al dimensions: 0.6 μm × 0.6 μm)
(Not to scale)

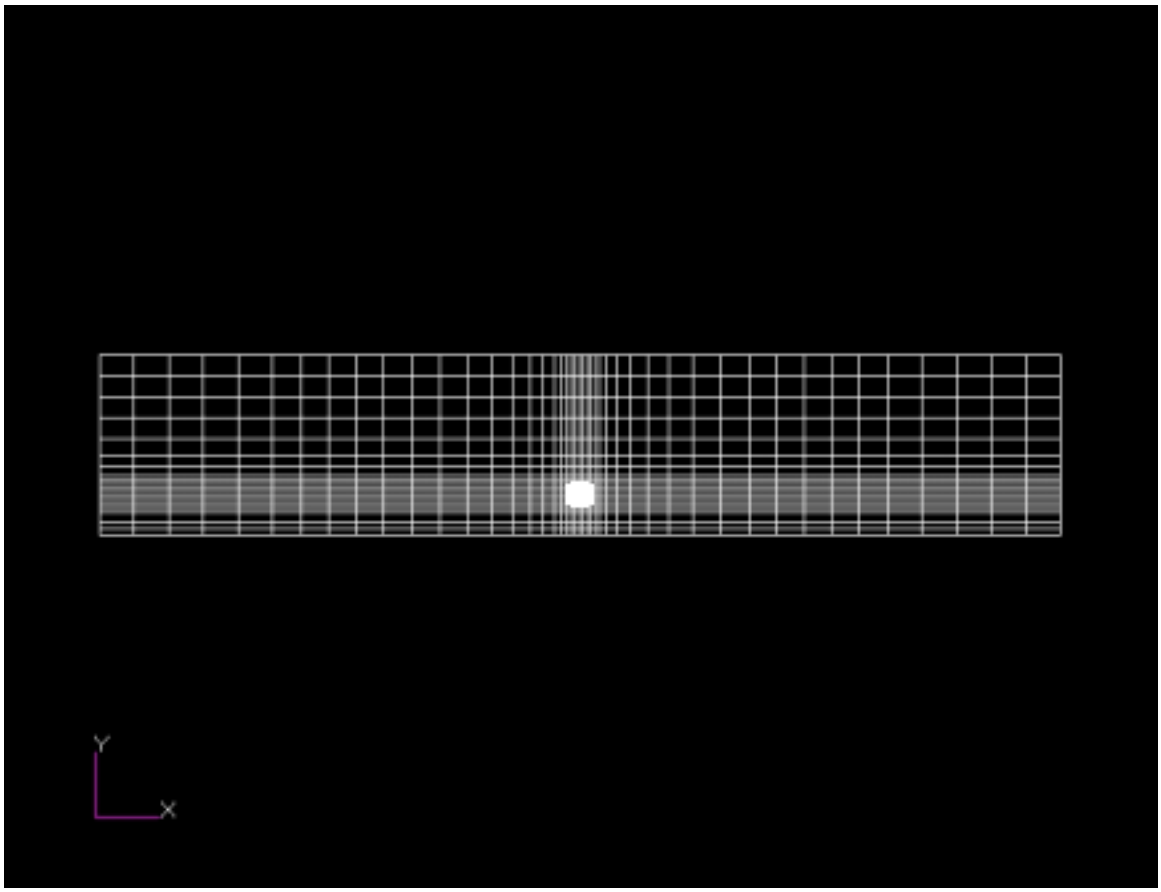


Fig. 2-1 Two-dimensional FEA model

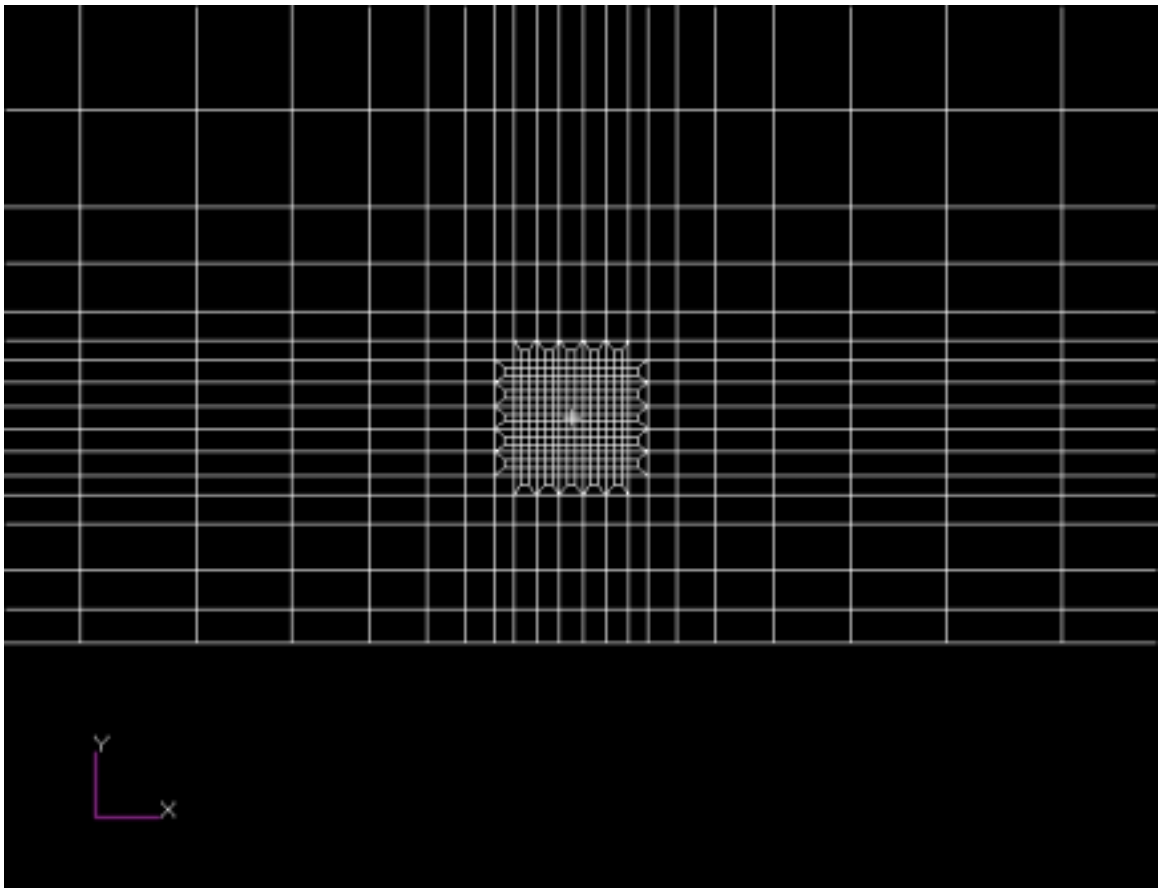


Fig. 3-1 Mesh details around the Al line

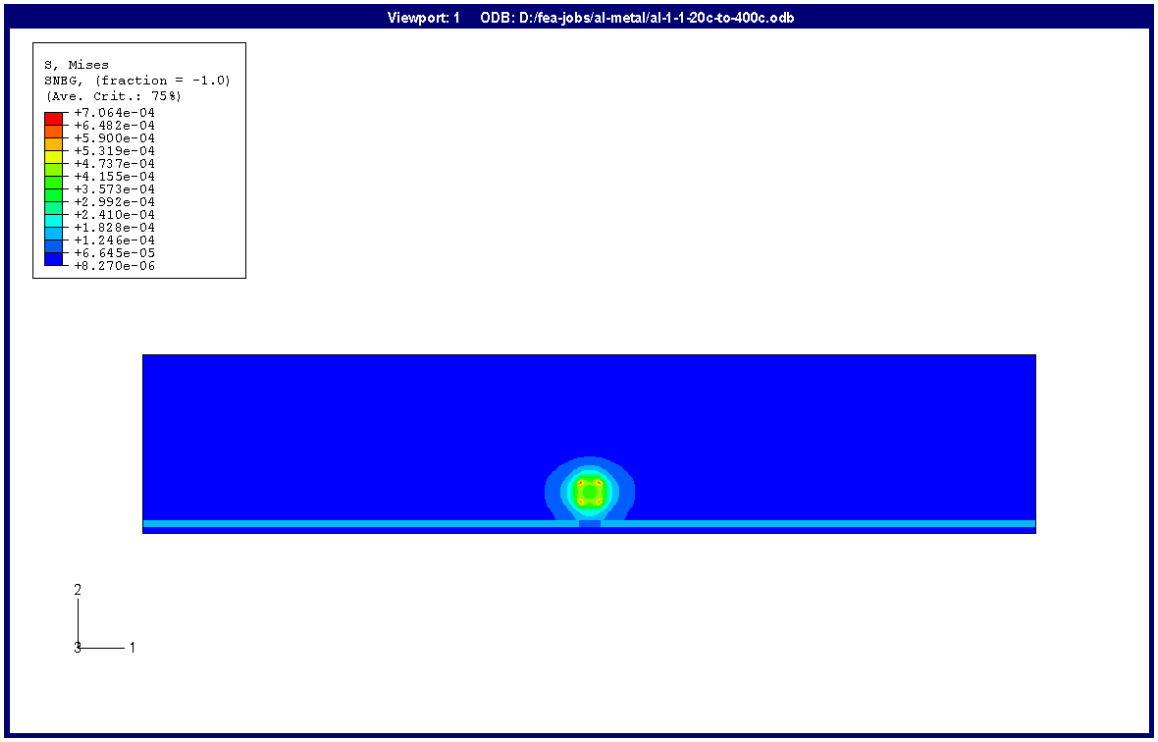


Fig. 4-1 Overall Von Mises stress distributions (20 °C to 400 °C)

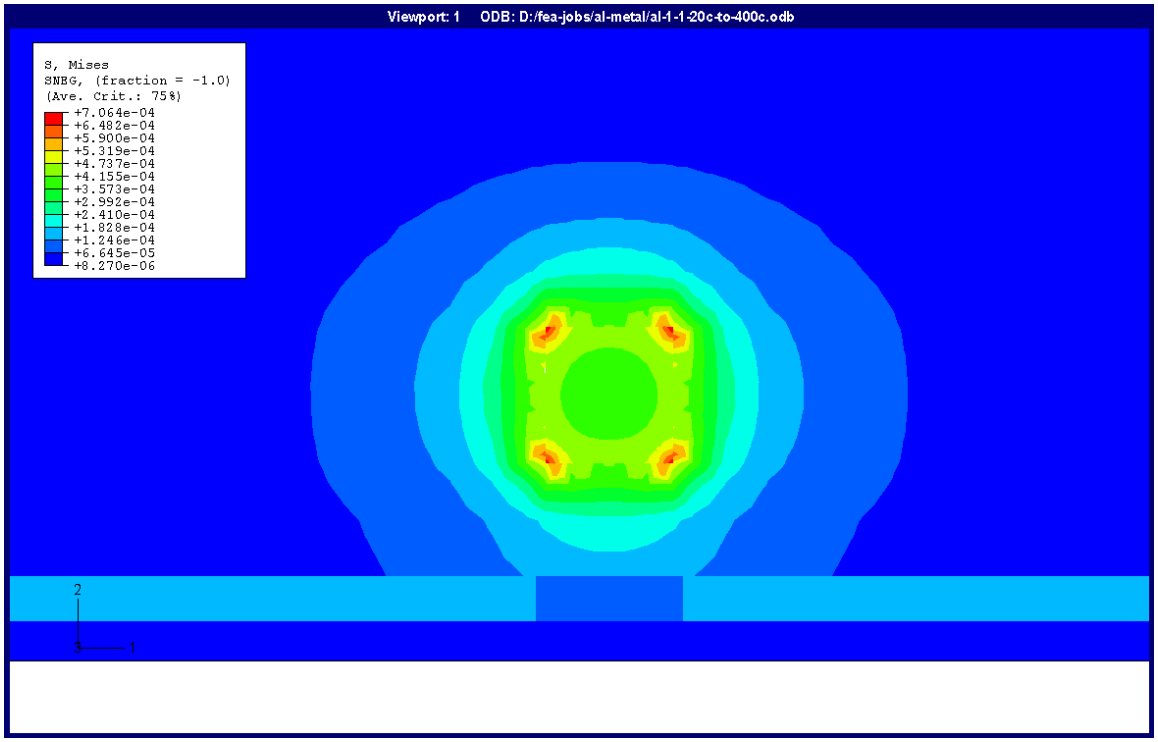


Fig. 5-1 Details of the Von Mises stress distribution in the Al vicinity (20 °C to 400 °C)

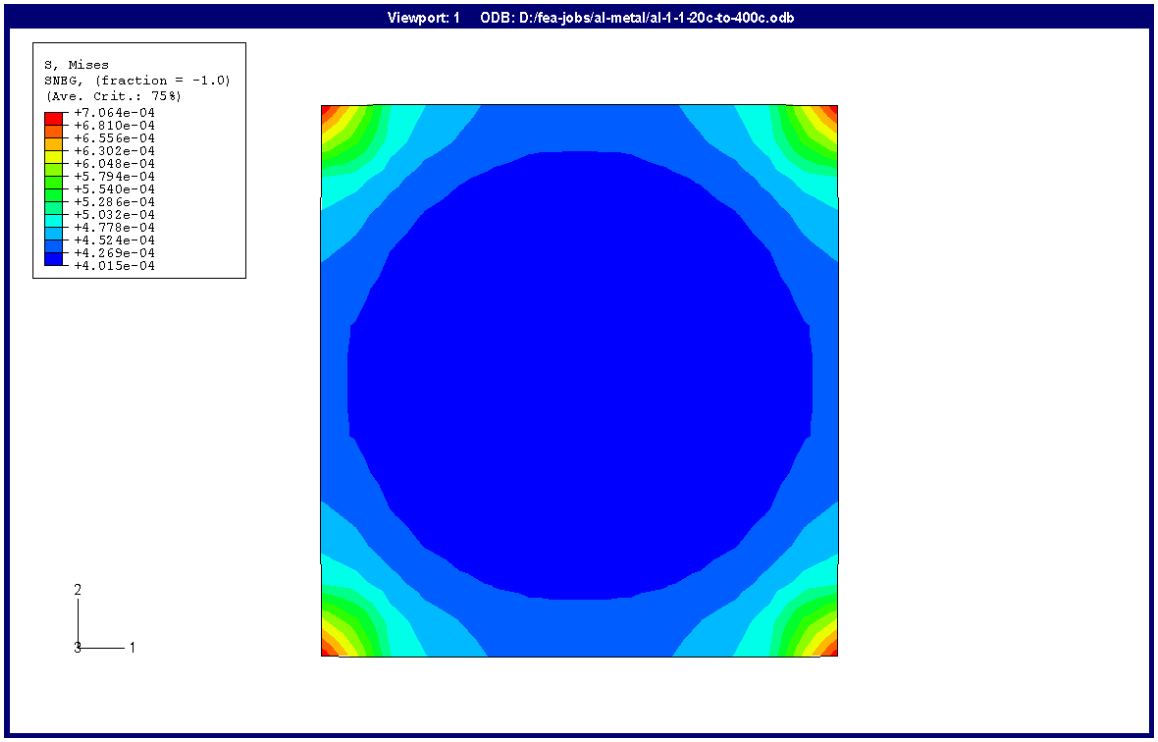


Fig. 6-1 Von Mises stress in the Al line (20 °C to 400 °C)

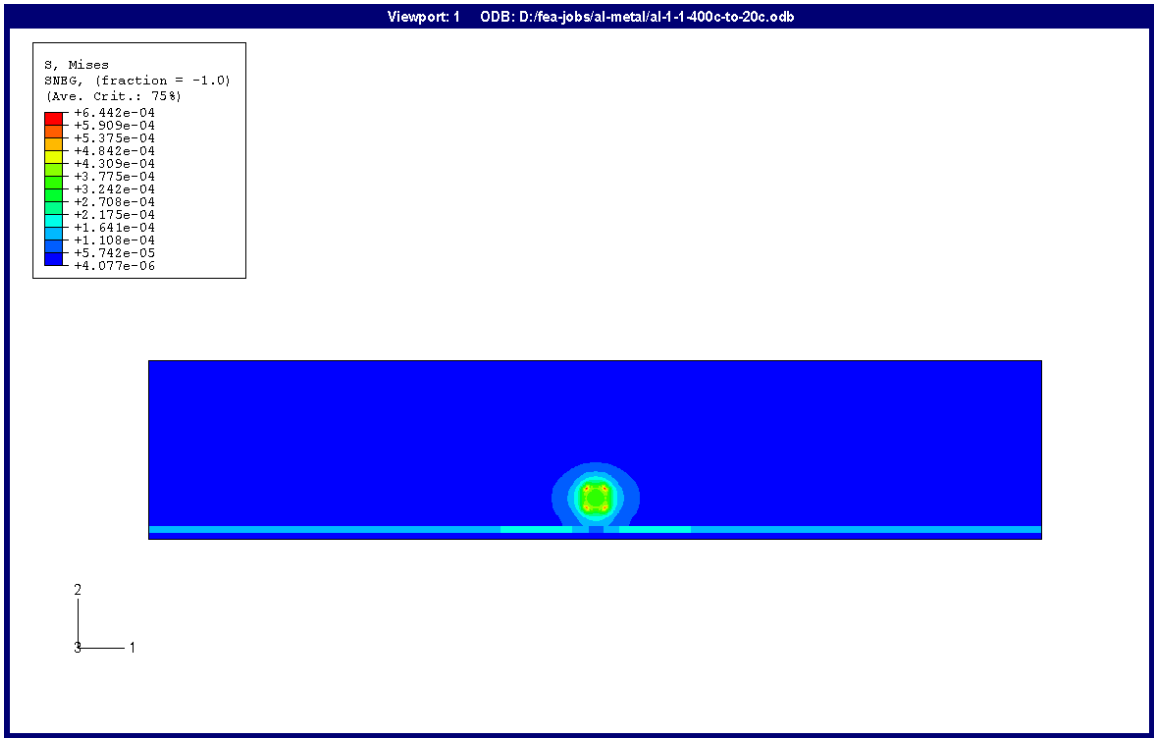


Fig. 7-1 Overall Von Mises stress distributions (400 °C to 20 °C)

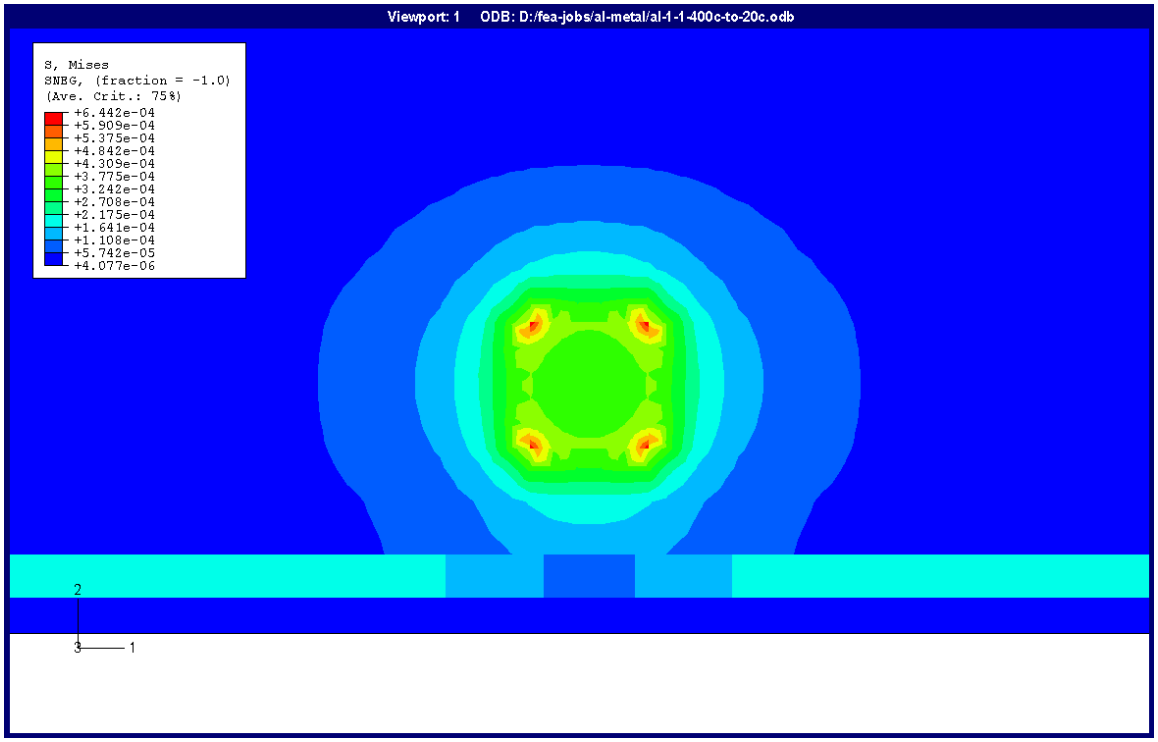


Fig. 8-1 Details of the Von Mises stress distribution in the Al vicinity (400 °C to 20 °C)

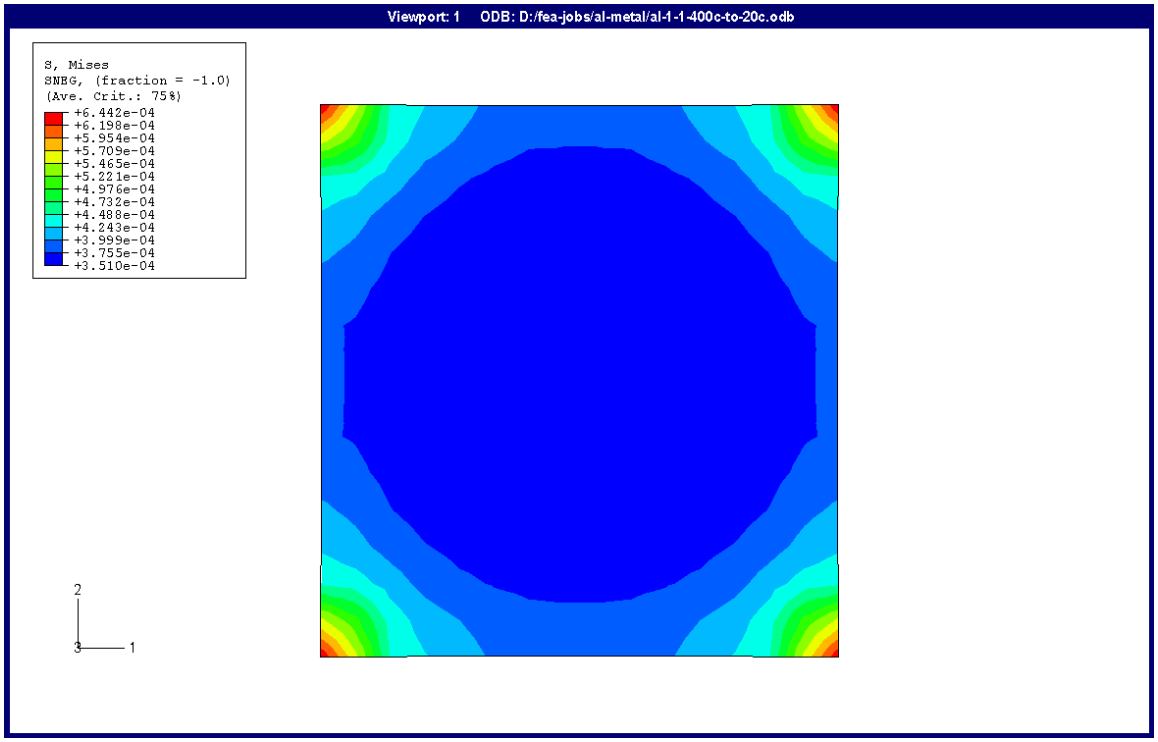


Fig. 9-1 Von Mises stress in the Al line (400 °C to 20 °C)

**Reliability Assessment of the Integrity of Aluminum Interconnect for a FDSOI Process using Finite Element Techniques**

**Part II – Heat Transfer Analysis**

## 1-2 Introduction

Heat transfer analysis for the Al-metallization study has been conducted. This part of the report summarizes the findings and results.

As has been mentioned in Part I, heat transfer analyses are performed based on the following conditions:

(i) the conduction is the only mode of heat transfer (scenario I);

(ii) natural convection and conduction are combined in the mode of heat transfer (scenario II);

(iii) both scenarios are based on a 0.1 A electric current flowing through the poly-Si strip;

## 2-2 Material Properties

Table 1-2 lists the thermal properties used for the analysis:

Table 1-2

| Materials | Thermal Conductivity (W/mK) |
|---|---|
| Si | 148 |
| Poly-Si | 148 |
| $SiO_2$ | 1.5 |

## 3-2 Analytical Results and Discussions

### 3-2-1 "Adiabatic-20" Boundary Conditions

Fig. 1-2 depicts the structure for the analysis. Note that the heat generation due to the electric current is concentrated in the poly-Si strip. In this cross-section model, the Al metal is not a part of the analysis due to the particular geometry of the device. The Al metal can be included in the FEA analysis only if the model is 3-D in nature. The 3-D analysis was also performed and will be discussed later in the report.

Figs. 2-2 and 3-2 show details of the 2-D finite element model. The following conditions are imposed for the heat transfer analysis:

(i) the bottom of the structure is held at 20 °C (room temperature);

(ii) the top of the structure is adiabatic;

(iii) the uniform power dissipation in the poly-silicon area is equivalent to a 0.1 A current flowing in the perpendicular direction;

Fig. 4-2 plots the temperature distribution in the whole structure. It is seen that the temperature ranges from the highest value of 94.8 °C in the poly-Si/$SiO_2$ area, to the

lowest value of 20 °C at the bottom of the structure. Fig. 5-2 shows an enlarged view in the poly-Si/$SiO_2$ area. To better view the detailed results, the temperature distributions inside the poly-Si and the $SiO_2$ are presented in Fig. 6-2 and Fig. 7-2 respectively. From Fig. 6-2, one can see that the temperature range in the poly-Si is from 82.6 °C at the both edges to 94.8 °C at the center of the strip, distributed symmetrically. Fig. 7-2 reveals that the range inside the $SiO_2$ is from 50.2 °C to 94.8 °C, also symmetrically distributed.

### 3-2-2 "20-20" Boundary Conditions

Another lab testing configuration imposes a 20 °C boundary condition at the top of the structure. Thus, the results presented in this section satisfy the following three conditions:

(i) the bottom of the structure is held at 20 °C;

(ii) the top of the structure is also held at 20 °C;

(iii) the uniform power dissipation in the poly-silicon area is equivalent to a 0.1 A current flowing in the perpendicular direction;

Fig. 8-2 shows the overall temperature distribution under the 20-20 boundary conditions. The highest temperature in the whole structure is shown to be 70.9 °C occurring in the poly-Si area (comparing with 94.8 °C under the adiabatic-20 boundary conditions). Because of the imposition of 20 °C at the top line that is very close to the heated area, the temperature gradient in that region is extremely high. Fig. 9-2 shows an enlarged view in that region of interest. Figs. 10-2 and 11-2 show the temperature distributions in the poly-si and in the $SiO_2$ respectively.

### 3-2-3 XY Plots

In fact, there exist temperature gradients within the tiny thickness (0.2 μm) of the poly-Si strip. The temperature fringe plots using color codes cannot reveal the gradients due to eye resolution issues. The only way to view the temperature variation is to utilize XY plots.

Fig. 12-2 plots the one-sided (symmetric) temperature variation between the bottom line and the top line of the poly-Si (only 0.2 μm apart) under the "adiabatic-20" conditions. Similar plot under the "20-20" conditions is shown in Fig. 13-2. These plots clearly reveal the temperature gradients along the thickness of the poly-Si strip. Interestingly, the temperature along the top line is higher than that along the bottom line in the case of "adiabatic-20", as the ultimate heat sink is at the bottom of the whole structure. However, this conclusion is reversed under the "20-20" conditions. This is obviously due to the fact that both the bottom as well as the top of the structure are the heat sinking interfaces.

Although the Al metallization is not represented by the shell-type finite elements in the 2-D analysis, we still have high interest in the temperature distribution along the "location of the Al metallization" (the geometric coordinates representing the cross-section location of the Al line perpendicular to the poly-Si strip). Since we know exactly the distance between the poly-si and the Al line, we can extract the temperature distribution at the Al location.

Fig. 14-2 plots the temperature variation along the Al line location, where the comparison is made between the "adiabatic-20" and the "20-20" thermal conditions. One can see clearly that the imposed "20-20" conditions have bought down the temperature significantly.

### 4.2 3-D Analysis and Discussions

As mentioned earlier, the 2-D FEA model does not include the Al metallization because the poly-Si and the Al line are arranged in a perpendicular fashion. The only way to include both of them in a single model is to perform a 3-D heat transfer analysis. In this section, the 3-dimensional analytical results are presented. A total of three cases have been analyzed:

Case 1: adiabatic conditions at the top, and heat sink (20 °C) at the bottom;

Case 2: heat sink (20 °C) at both the top and the bottom;

Case 3: natural convection at the top, and heat sink (20 °C) at the bottom;

The 3-D FEA model is shown in Fig. 15-2. This model represents a "cut-out" element (500 μm × 500 μm) from the whole device.

Figs. 16-2 through 21-2 show the 3-D temperature distributions along the Al metallization under the three cases. Their numerical values are to be examined in the XY plots below.

To better view the temperature distributions, XY plots are presented in Figs. 22-2 (case 1), 23-2 (case 2), and 24-2 (case 3).

In the first case, the highest temperature is 75.6 °C, compared to the 2-D result which is 94.8 °C. Several reasons can be explained for this difference. First, 2-D heat transfer analysis tends to overestimate the thermal resistance along the conduction paths and produce higher than actual temperature readings. This is because the effect of 3-D heat flux field distribution is not reflected in any 2-D analysis assumptions. Secondly, the

results for the Al metallization from the 2-D analysis are obtained using "Al metallization location" extraction instead of using actual finite elements. This would inevitably introduce errors. Thirdly, using 3-D "cut-out" element with a dimension of 500 μm × 500 μm to represent the 3-D whole device is itself an approximation, and the overall temperature is brought down to certain extent by the bottom heat sink (20 °C) because of its small-than-actual geometries. Thus it is believed that the highest temperature of the Al should be somewhere between 80 °C and 90 °C.

Similar observations are made with the "20-20" boundary conditions (the second case), where the highest Al temperature is about 48 °C (vs. 57 °C in the 2-D results). The explanations above should apply here as well.

Natural convection at the top of the model is confirmed in the third case to have a very minor role in reducing Al metal temperature. For a flat slab, typical heat transfer coefficient under natural convection condition is in the range from 10 $W/m^2C$ to 48 $W/m^2C$ depending on the experimental set-up. Using 10 yielded virtually the same result as in case 1 (adiabatic condition at the top).

The results shown in Figs. 20-1, 21-2 and 24-2 were obtained using 48 $W/m^2C$, the best case for natural convection. It can only reduce the highest temperature of Al metal by slightly more than 1 C. This has also validated many electronic packaging related thermal analyses where natural convection effects are completely ignored.

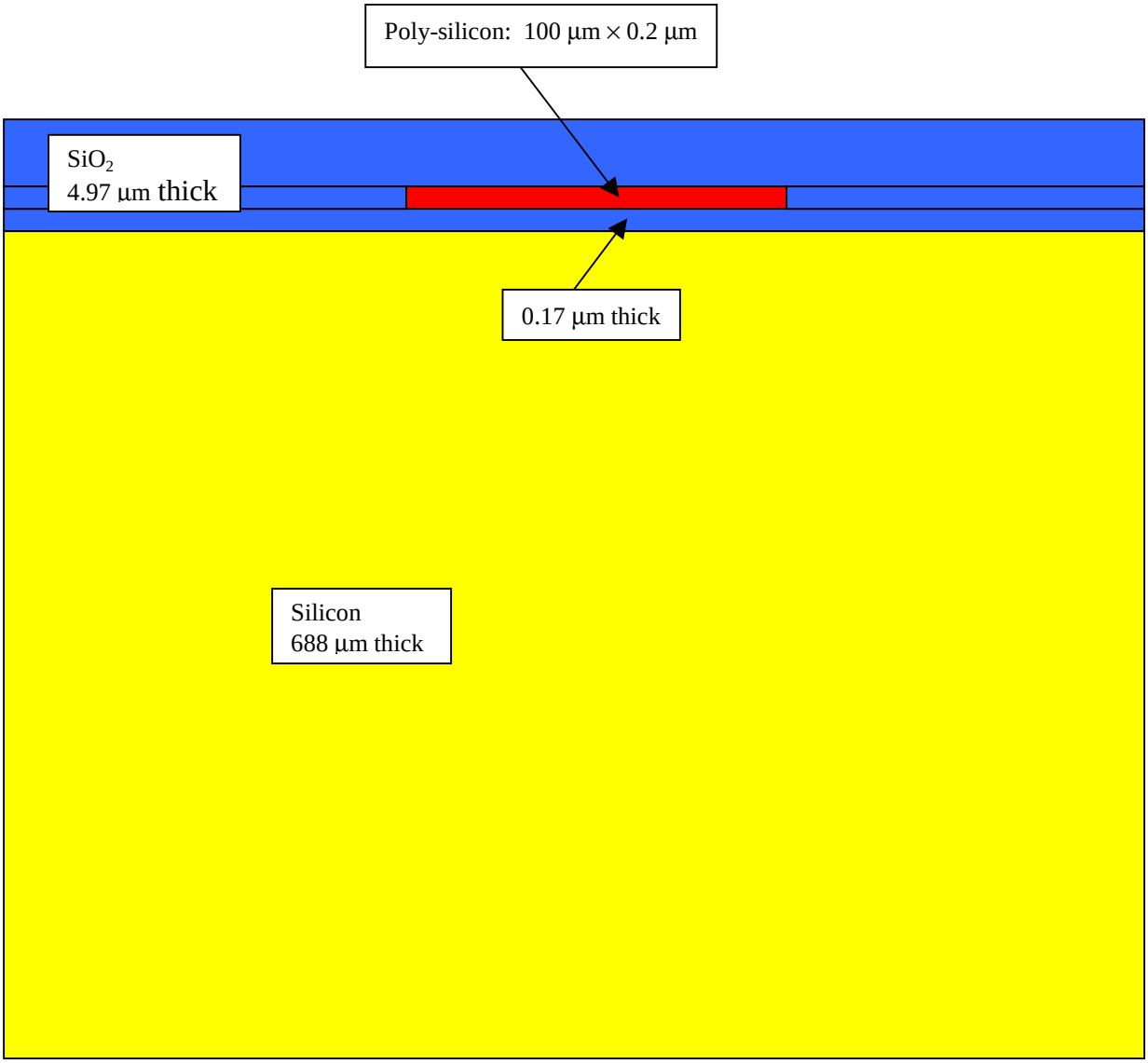


Fig. 1-2 The structure for heat transfer analysis (not to scale)

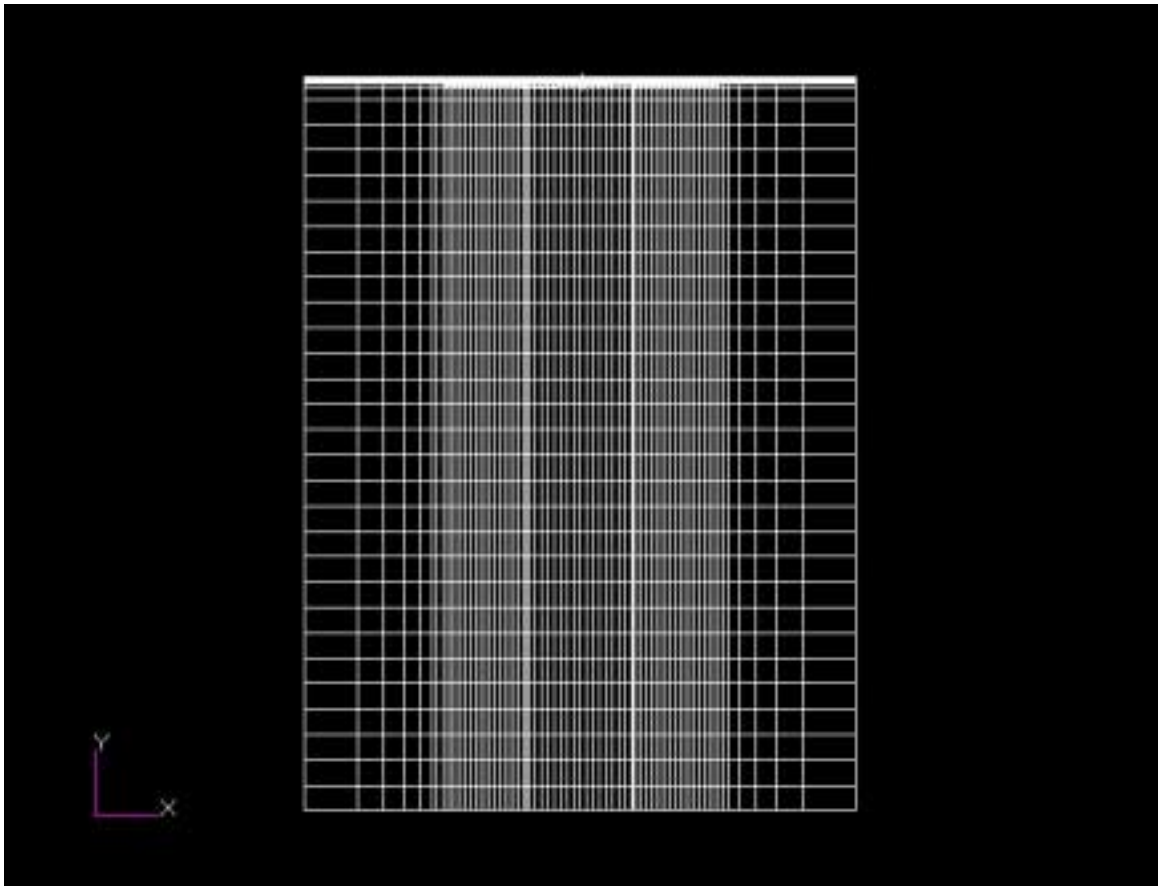


Fig. 2-2 Whole FEA mesh

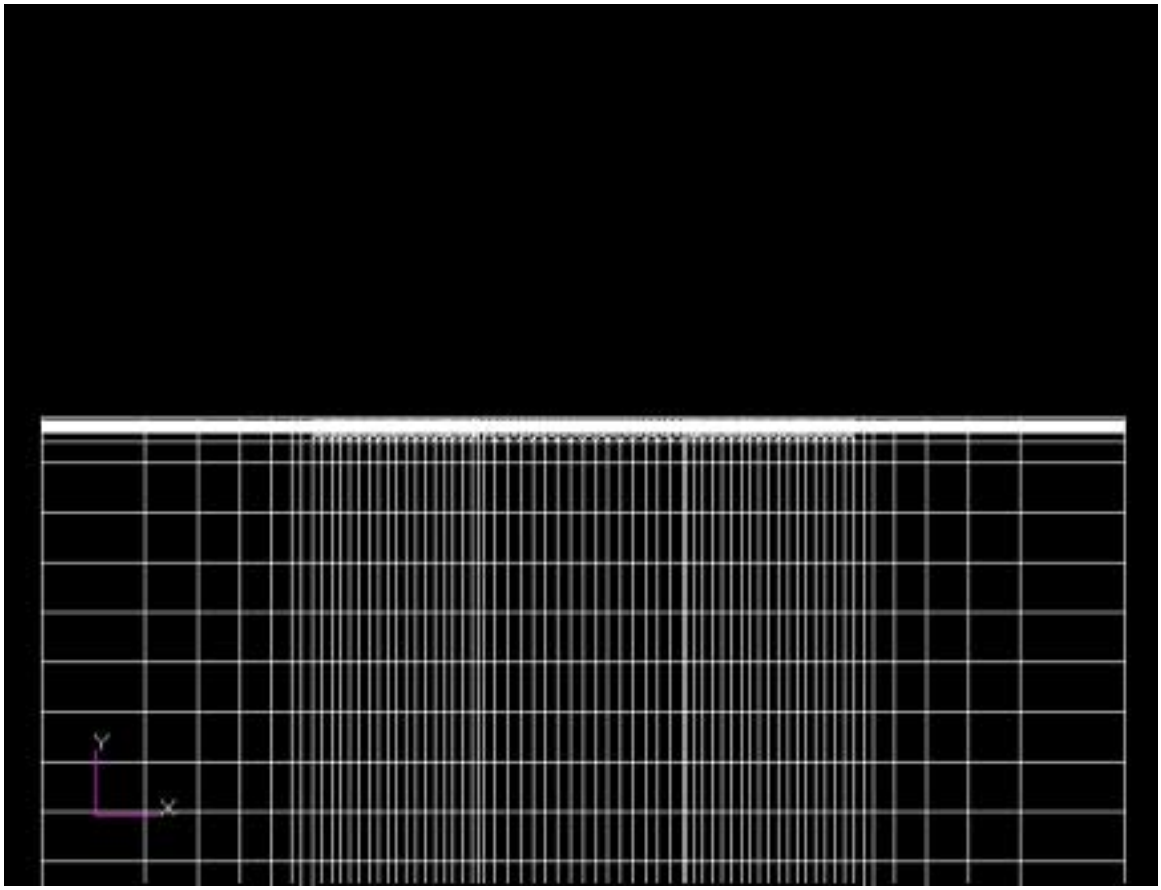


Fig. 3-2 Detailed FEA mesh near the heated area

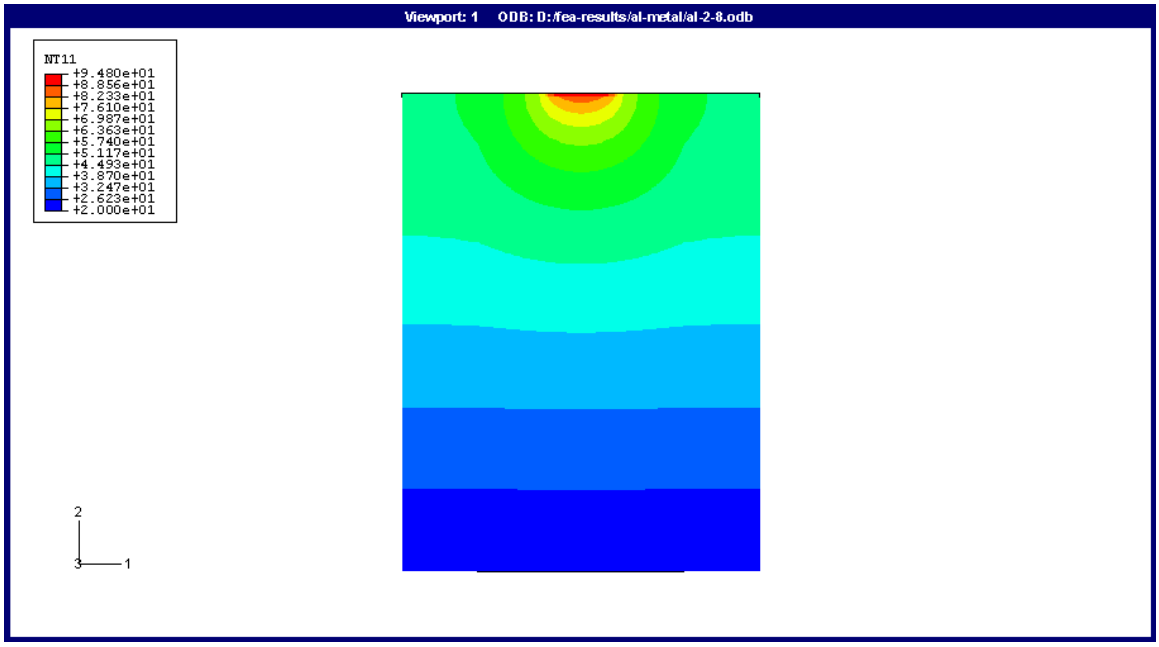


Fig. 4-2 Temperature distribution

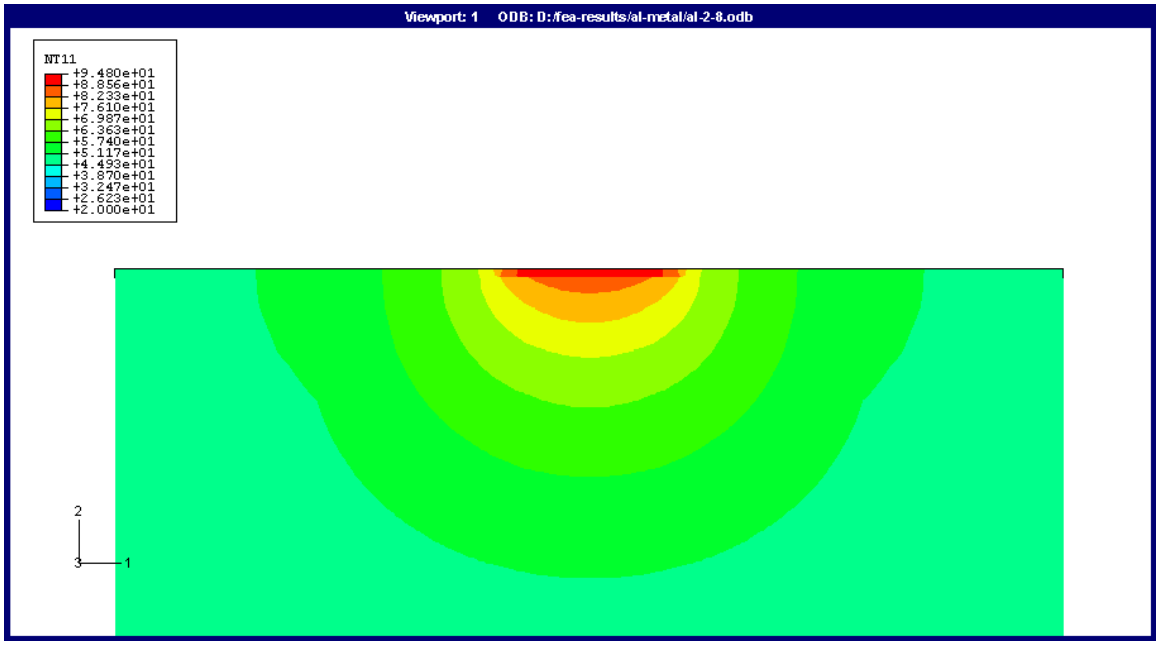


Fig. 5-2 Temperature distribution (detailed view near the heated area)

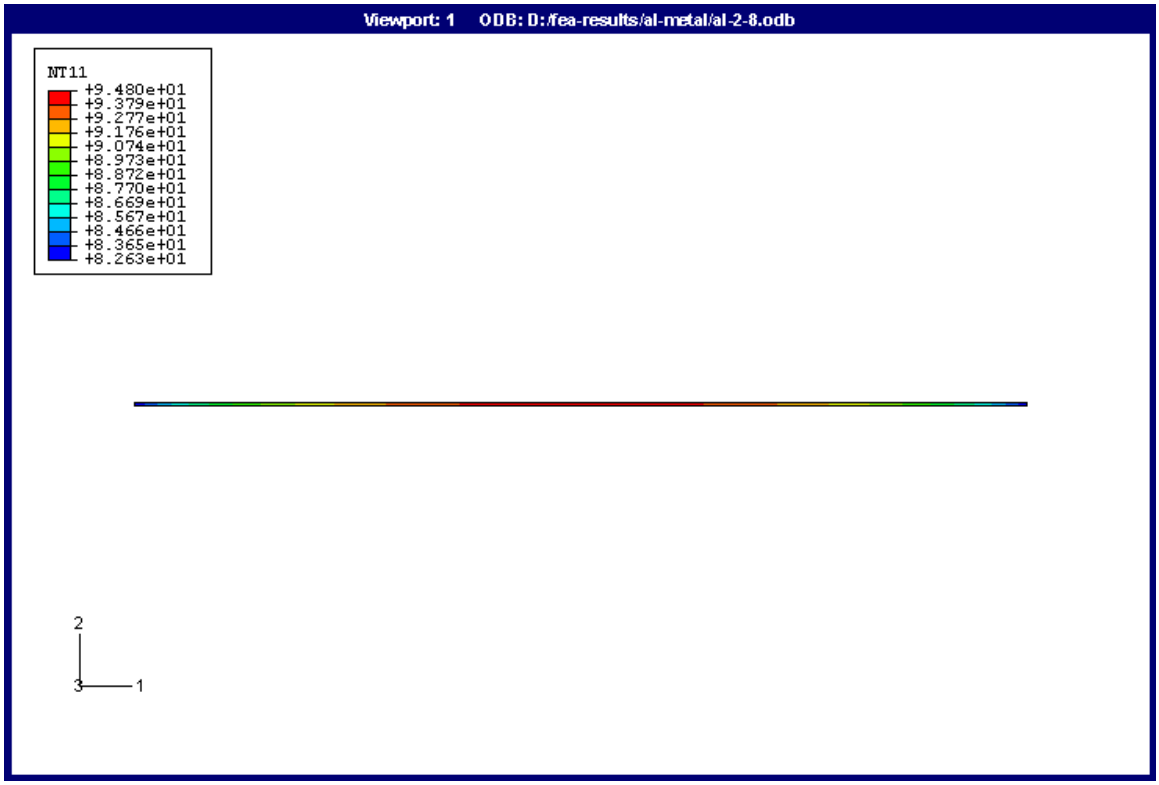


Fig. 6-2 Temperature distribution in the poly-silicon strip

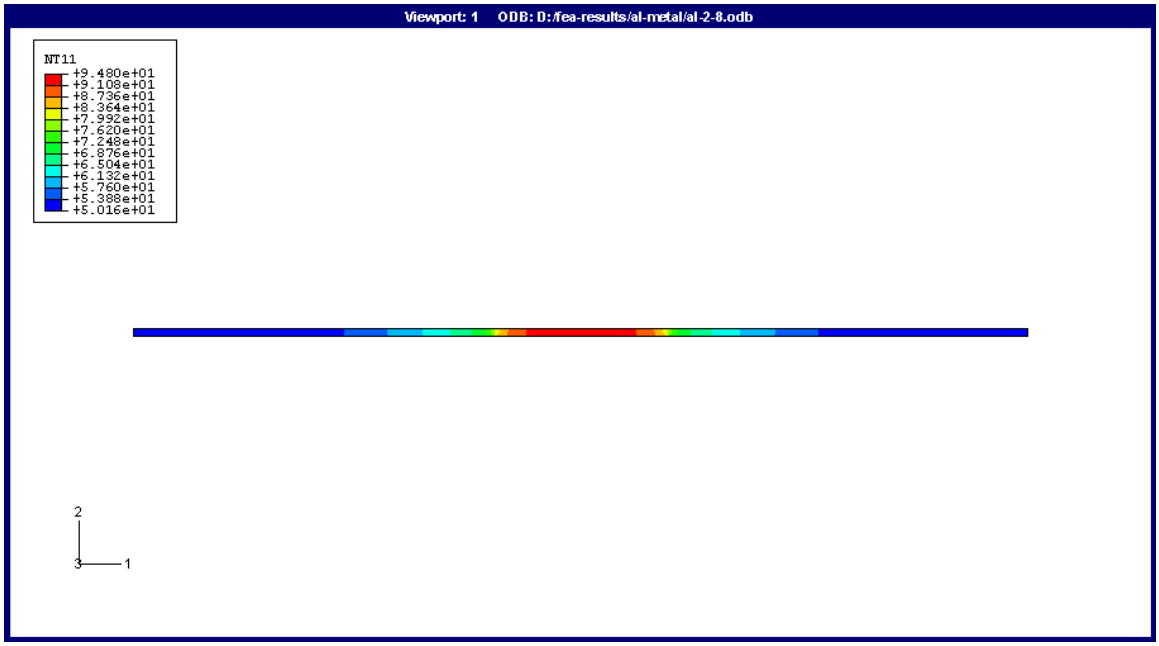


Fig. 7-2 Temperature distribution in the $SiO_2$

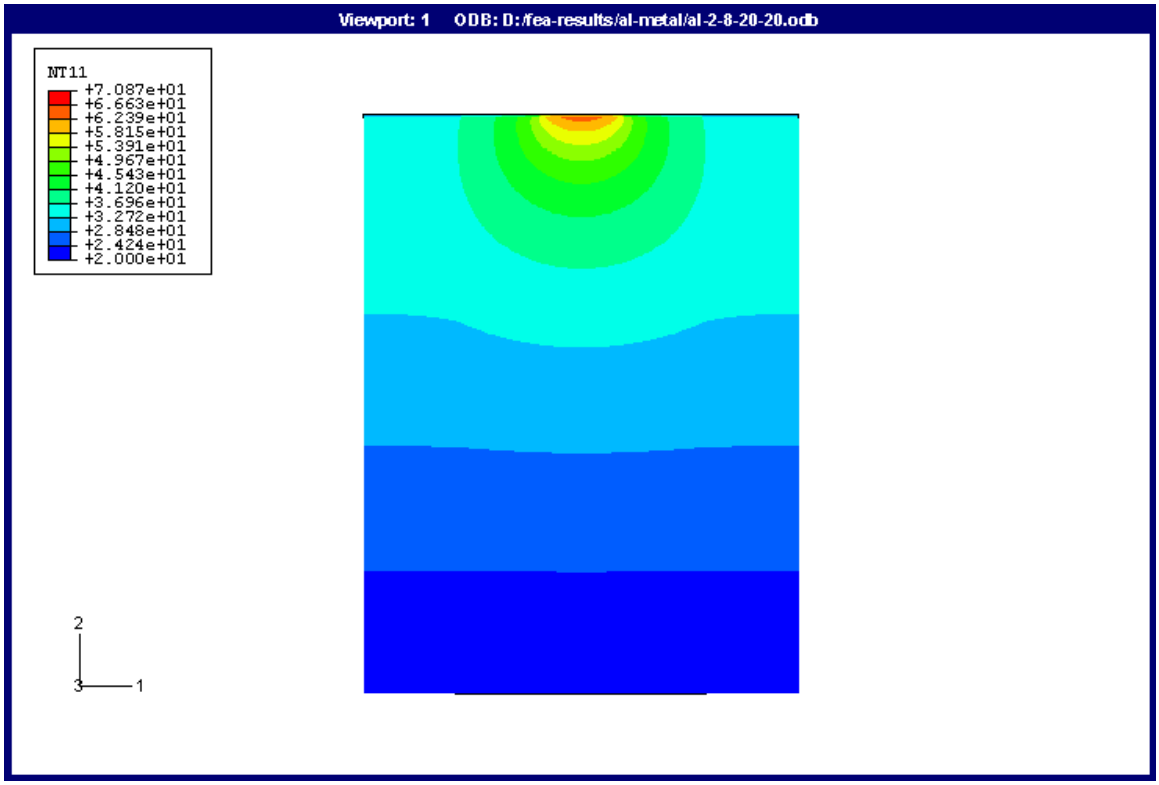


Fig. 8-2 Temperature distribution (20-20)

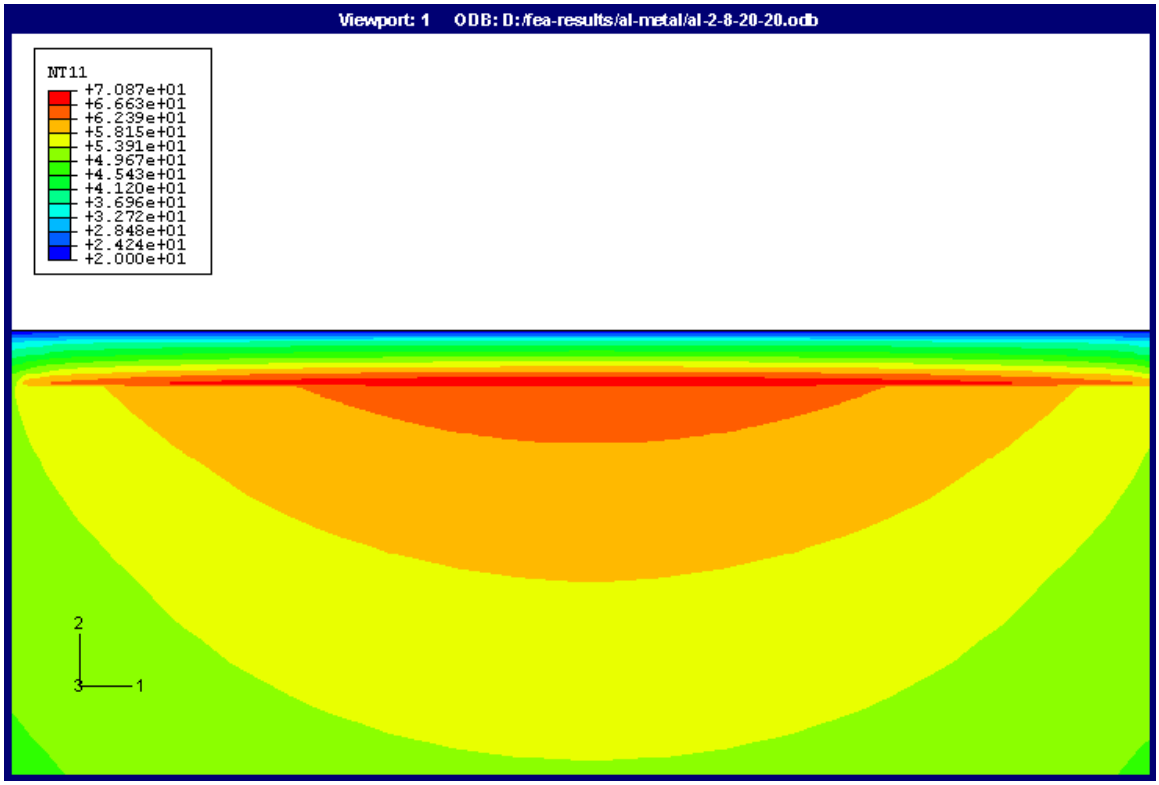


Fig. 9-2 Temperature distribution (20-20, detailed view in the heated area)

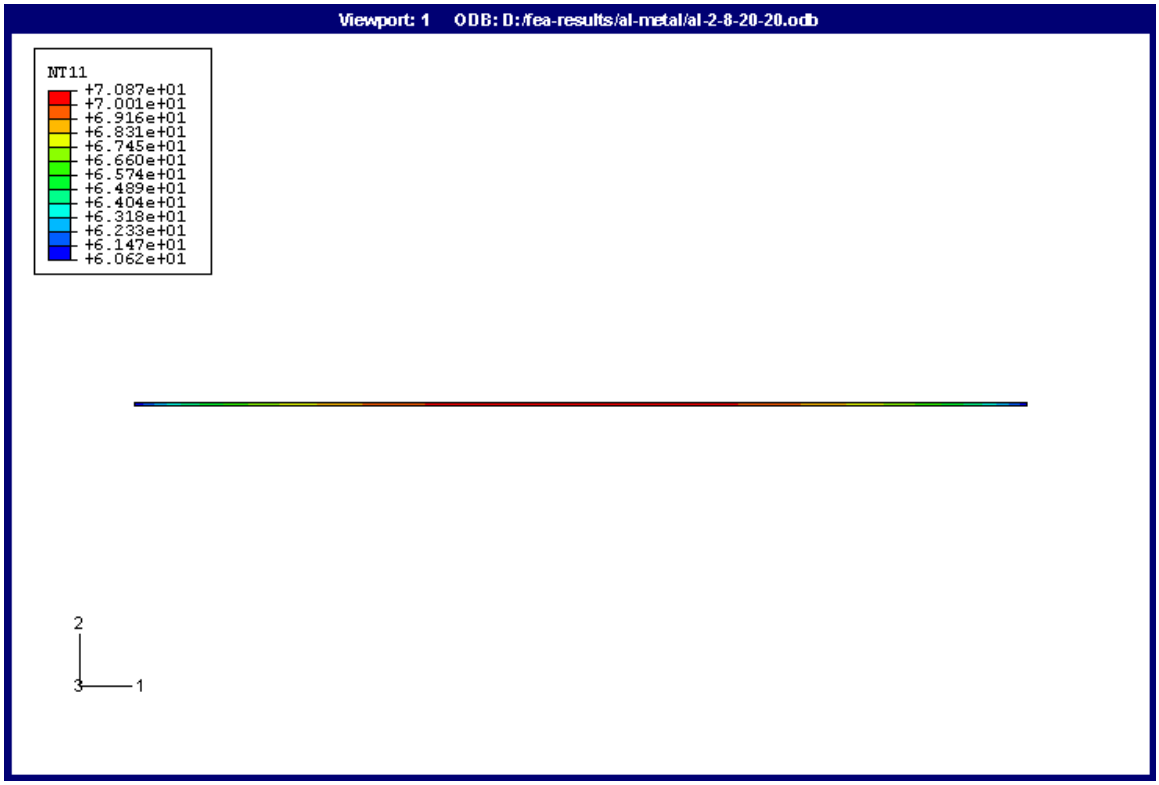


Fig. 10-2 Temperature distribution in the poly-silicon strip (20-20)

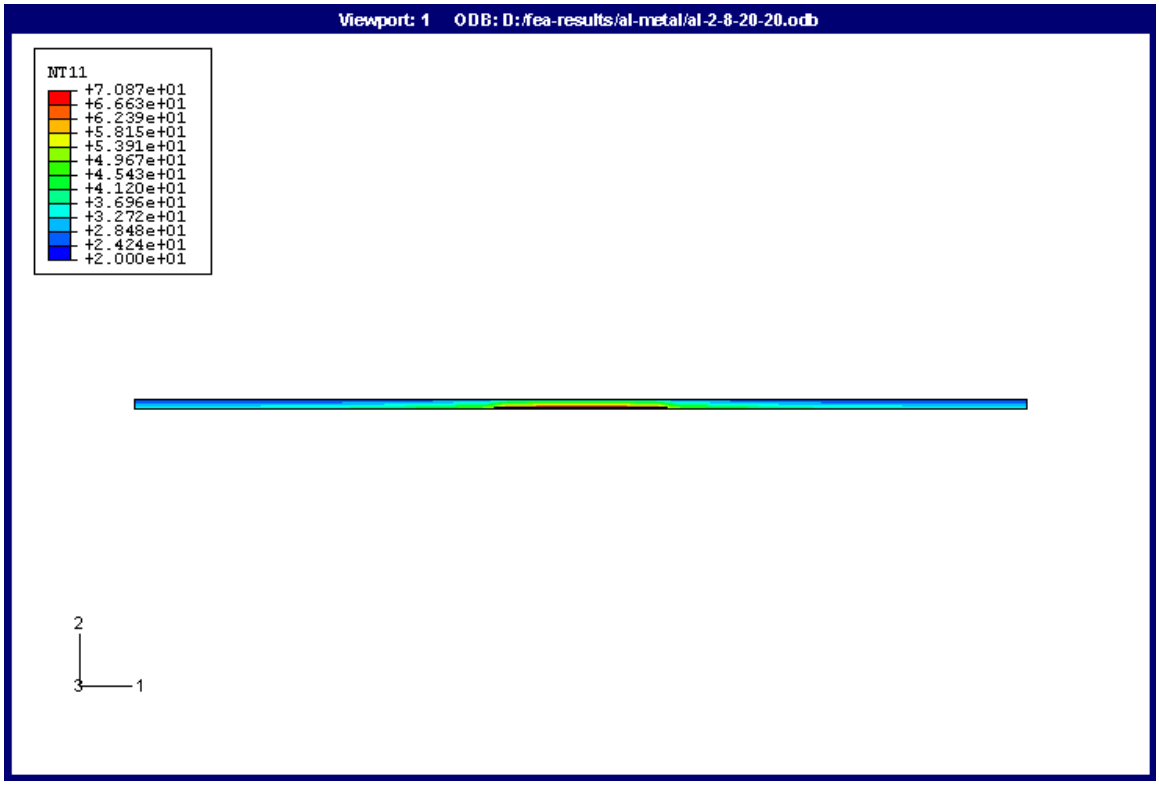


Fig. 11-2 Temperature distribution in the $SiO_2$ (20-20)

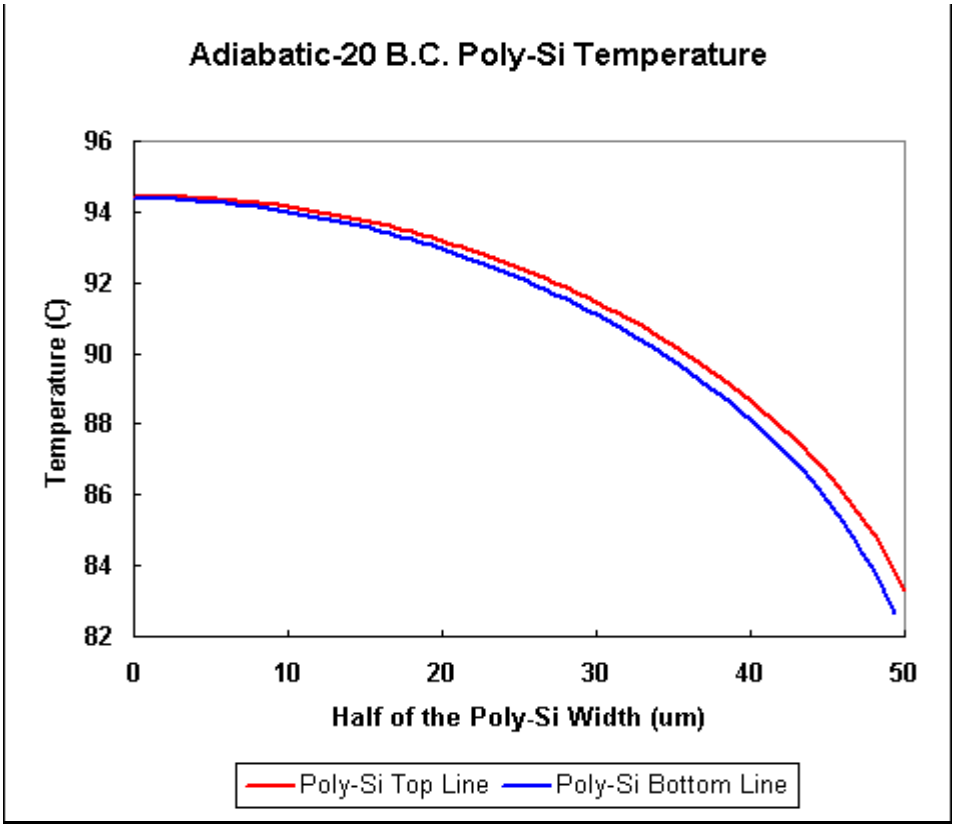


Fig. 12-2 Temperature gradients within the poly-Si thickness (adiabatic-20)

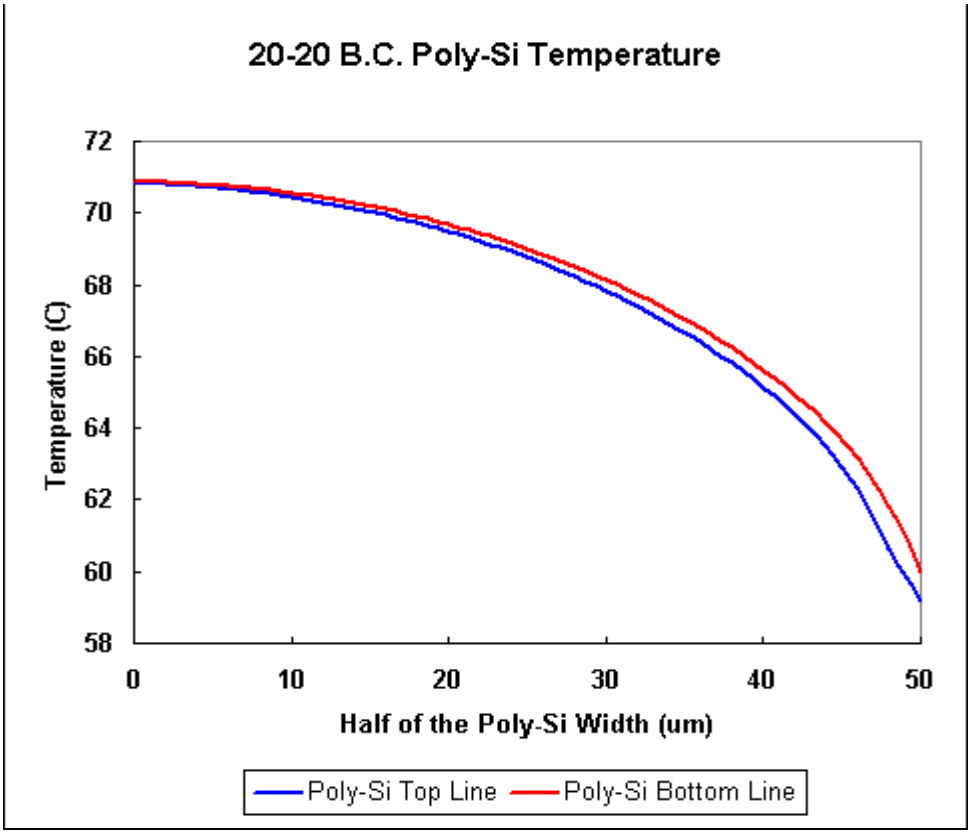


Fig. 13-2 Temperature gradients within the poly-Si thickness (20-20)

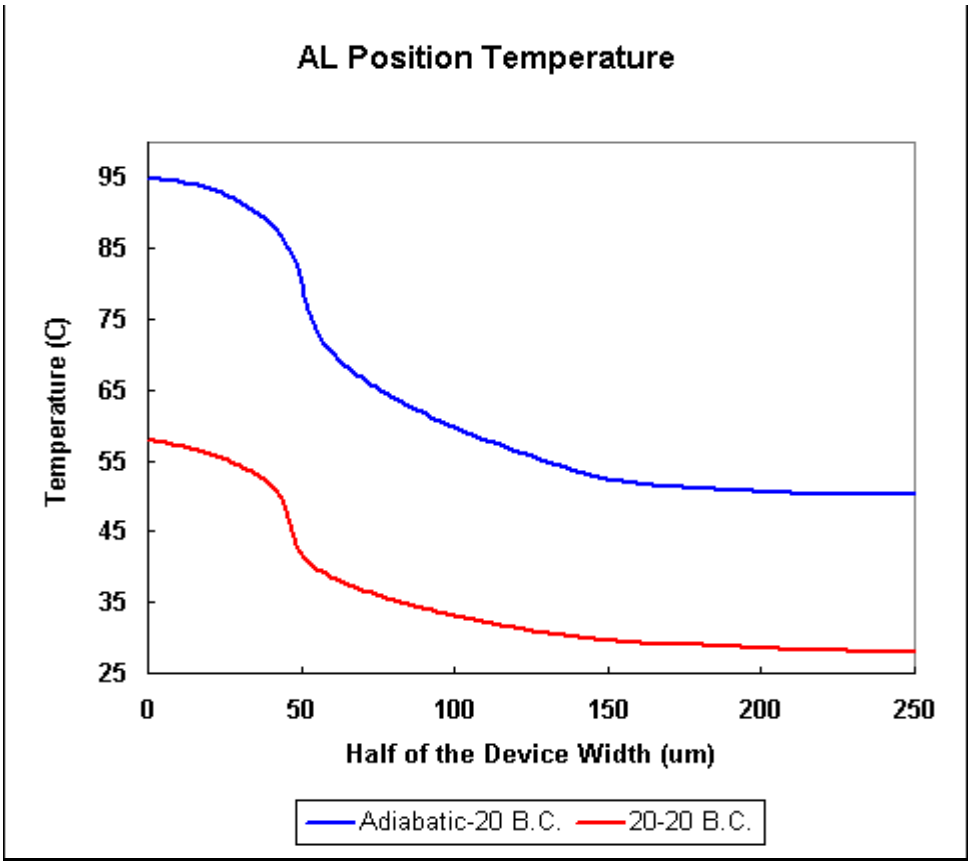


Fig. 14-2 Temperature along “Al location”

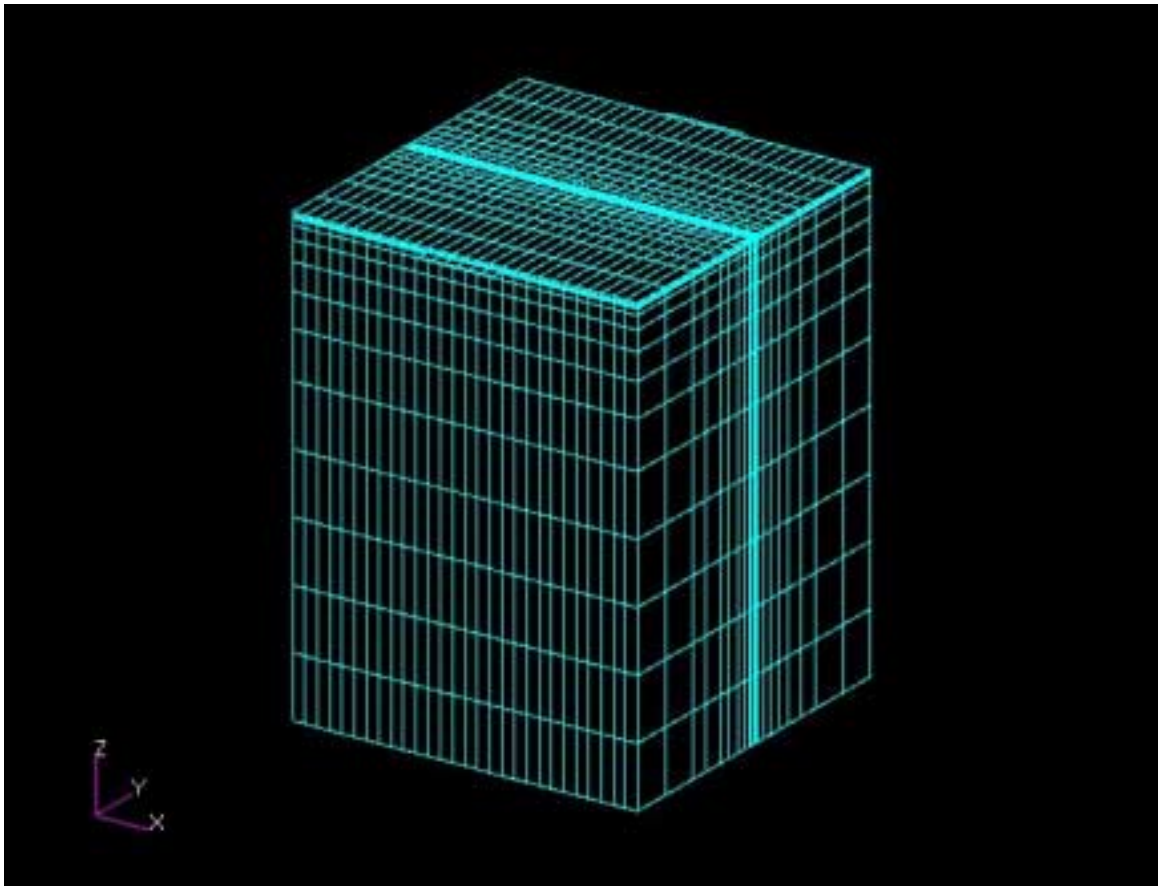


Fig. 15-2 3-D FEA model

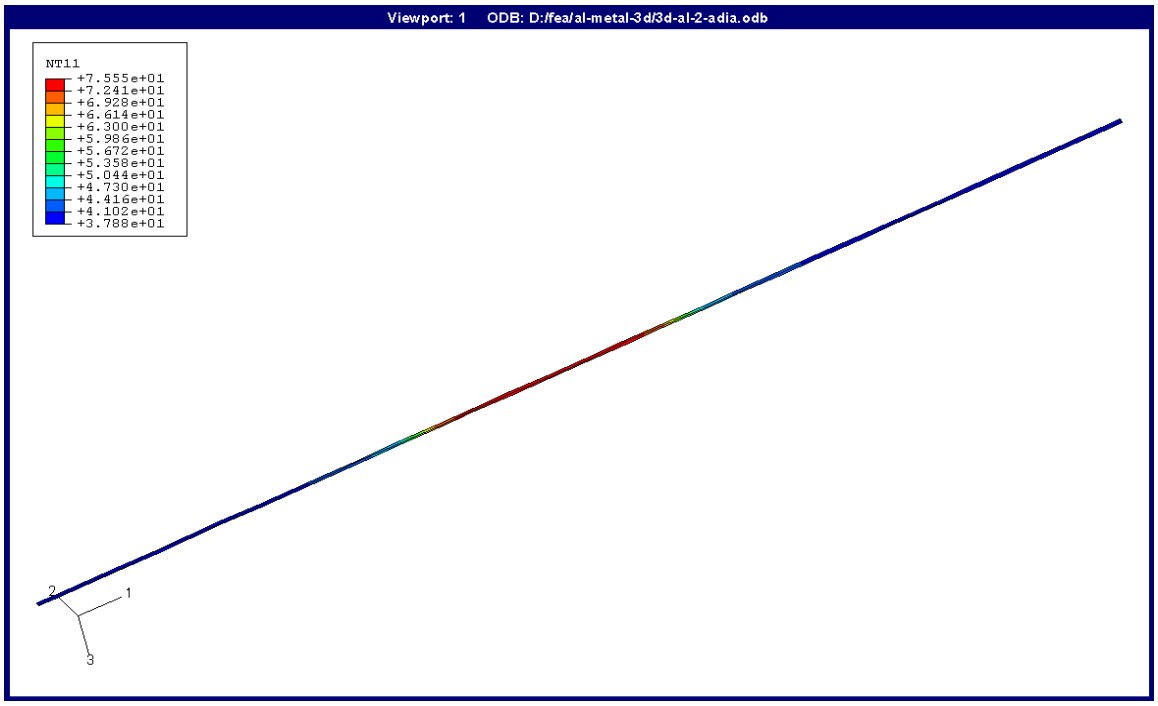


Fig. 16-2 Temperature in the Al metal (case 1)

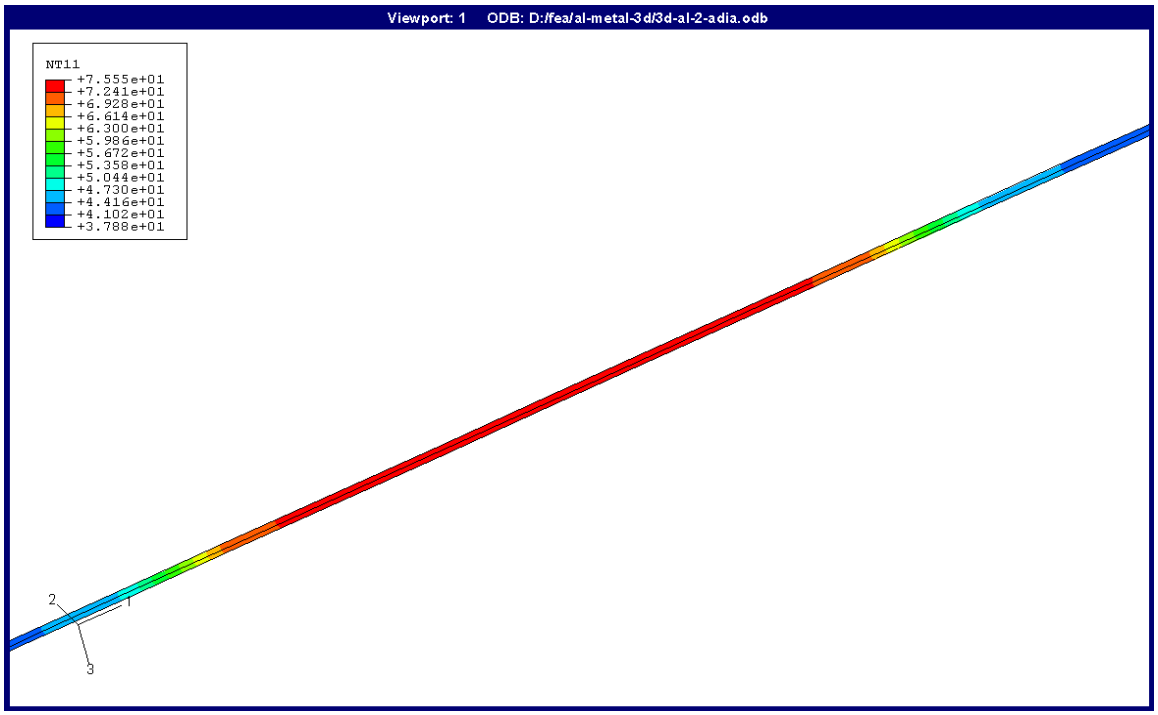


Fig. 17-2 Temperature in the Al metal—detailed view (case 1)

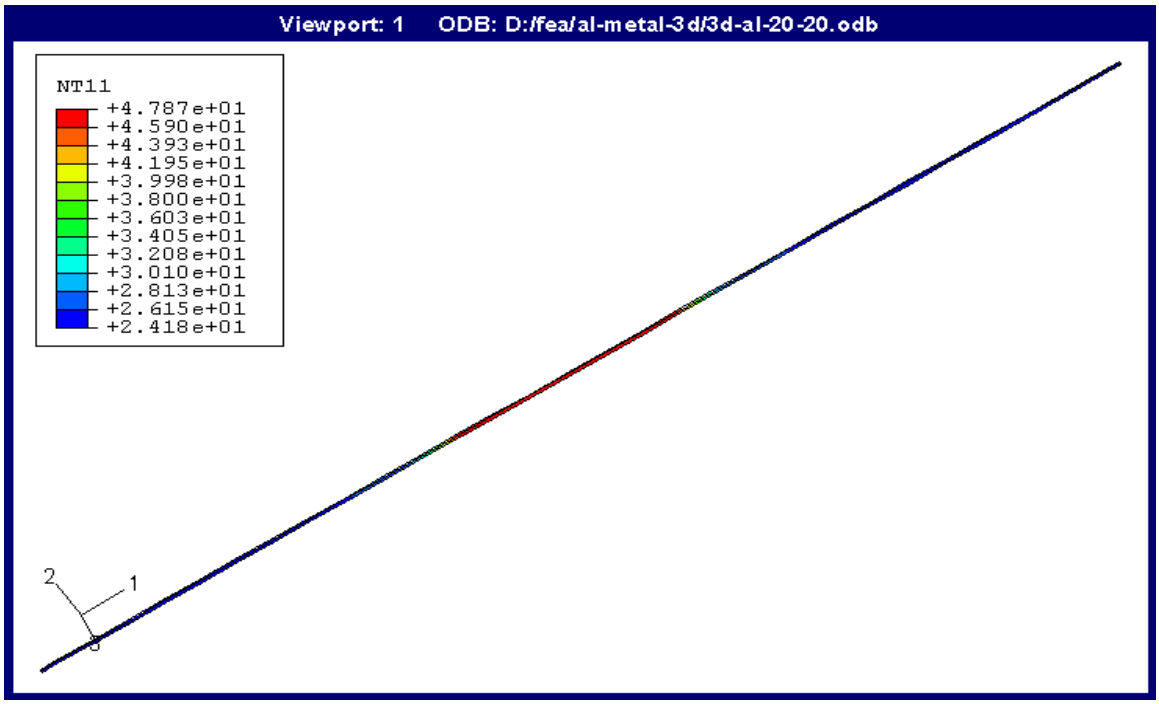


Fig. 18-2 Temperature in the Al metal (case 2)

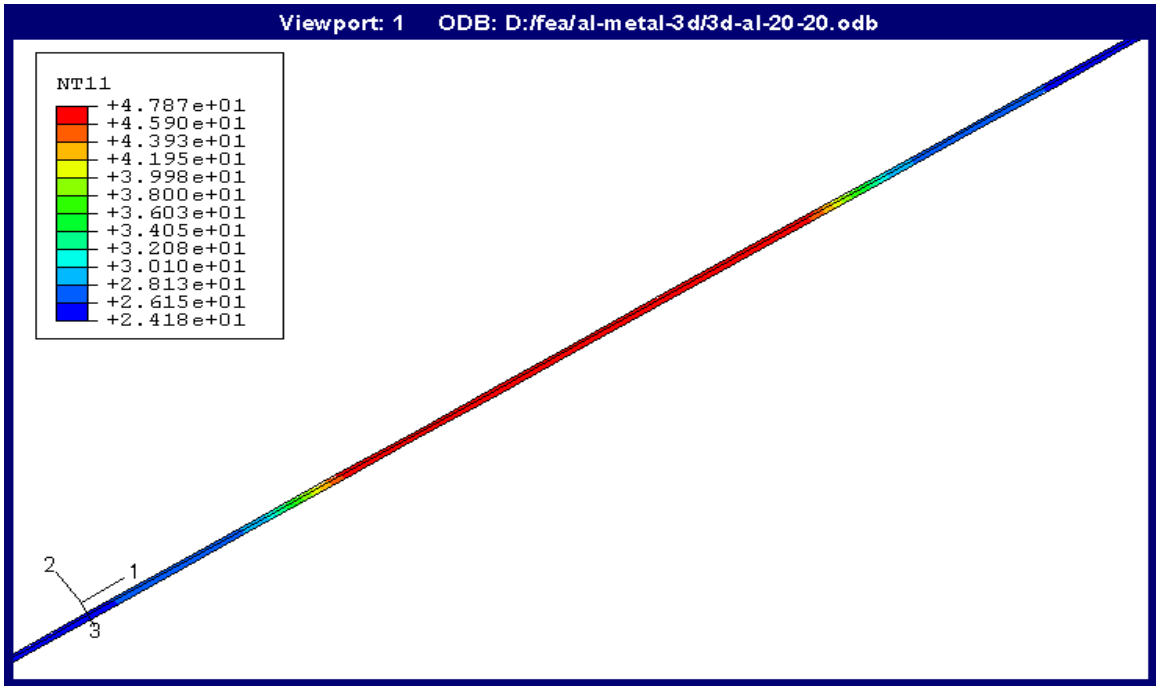


Fig. 19-2 Temperature in the Al metal—detailed view (case 2)

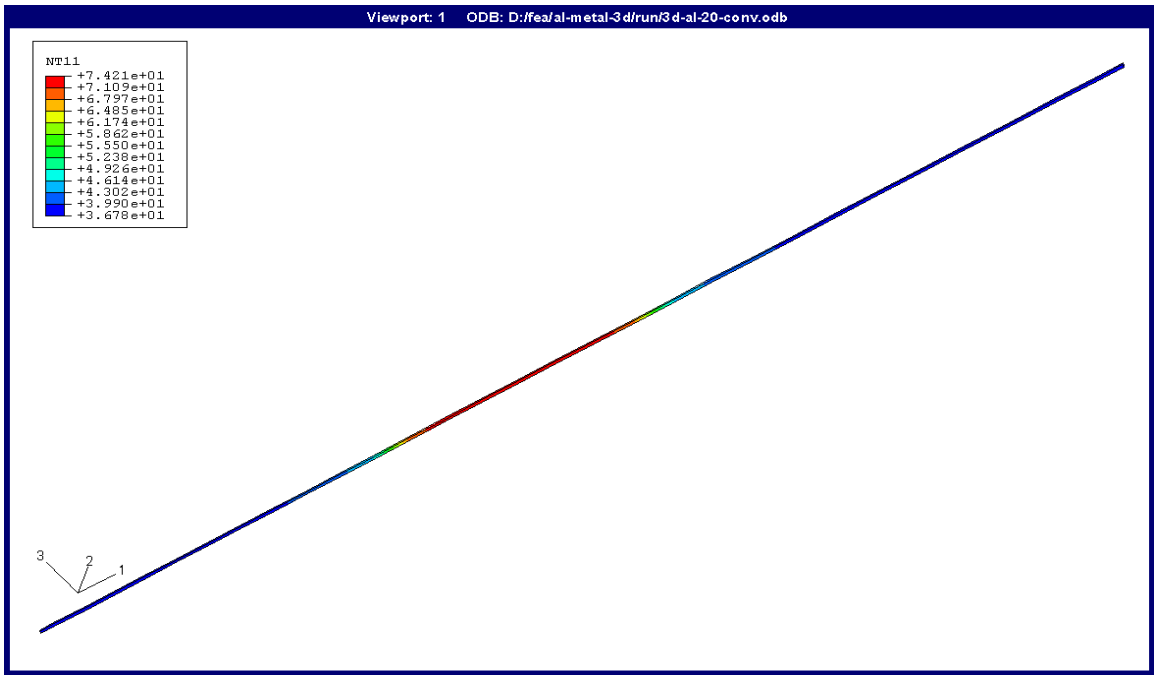


Fig. 20-2 Temperature in the Al metal (case 3)

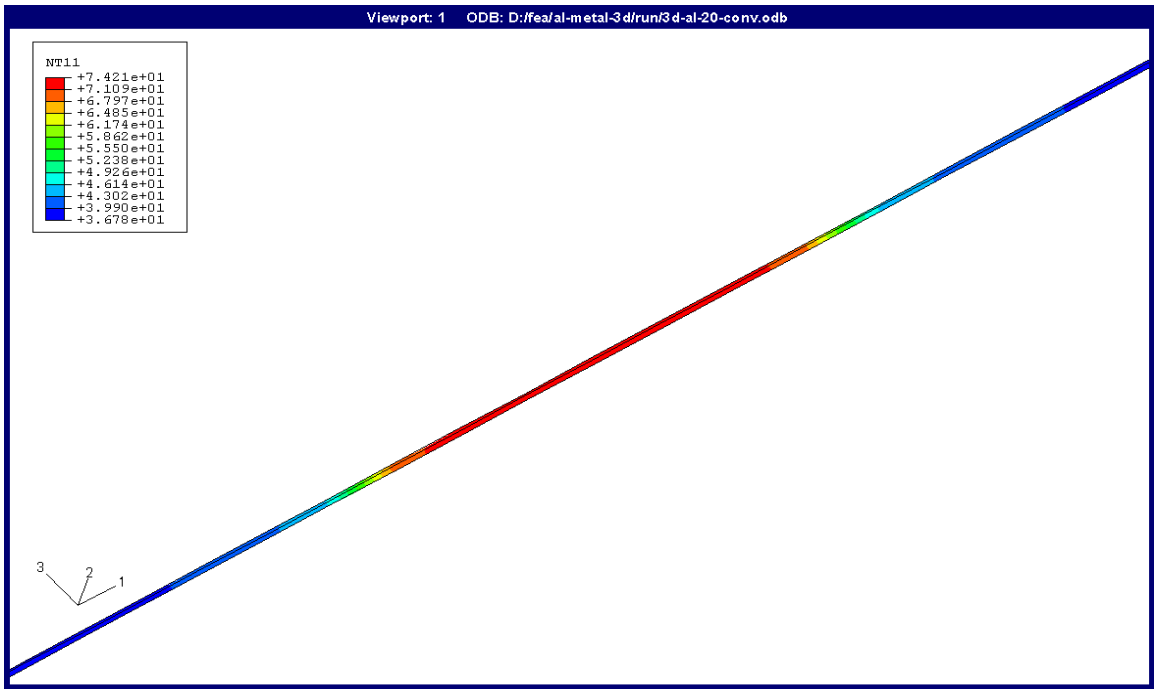


Fig. 21-2 Temperature in the Al metal—detailed view (case 3)

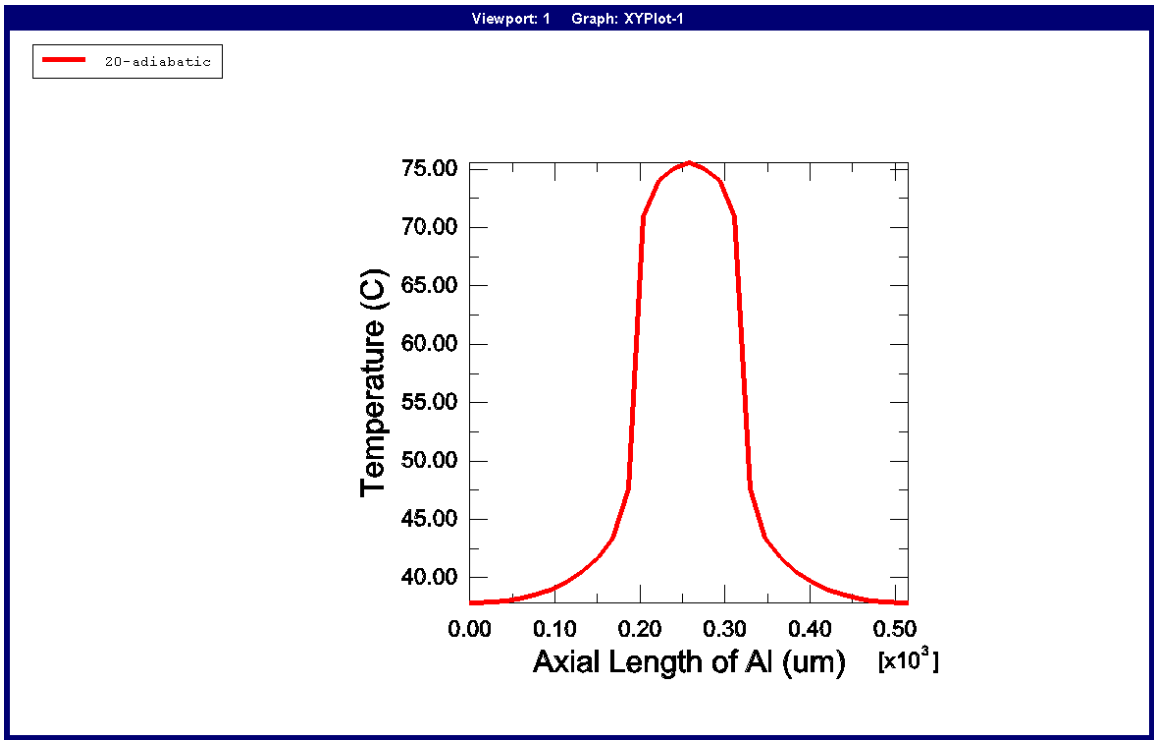


Fig. 22-2 XY plot of axial temperature distribution in Al (case 1)

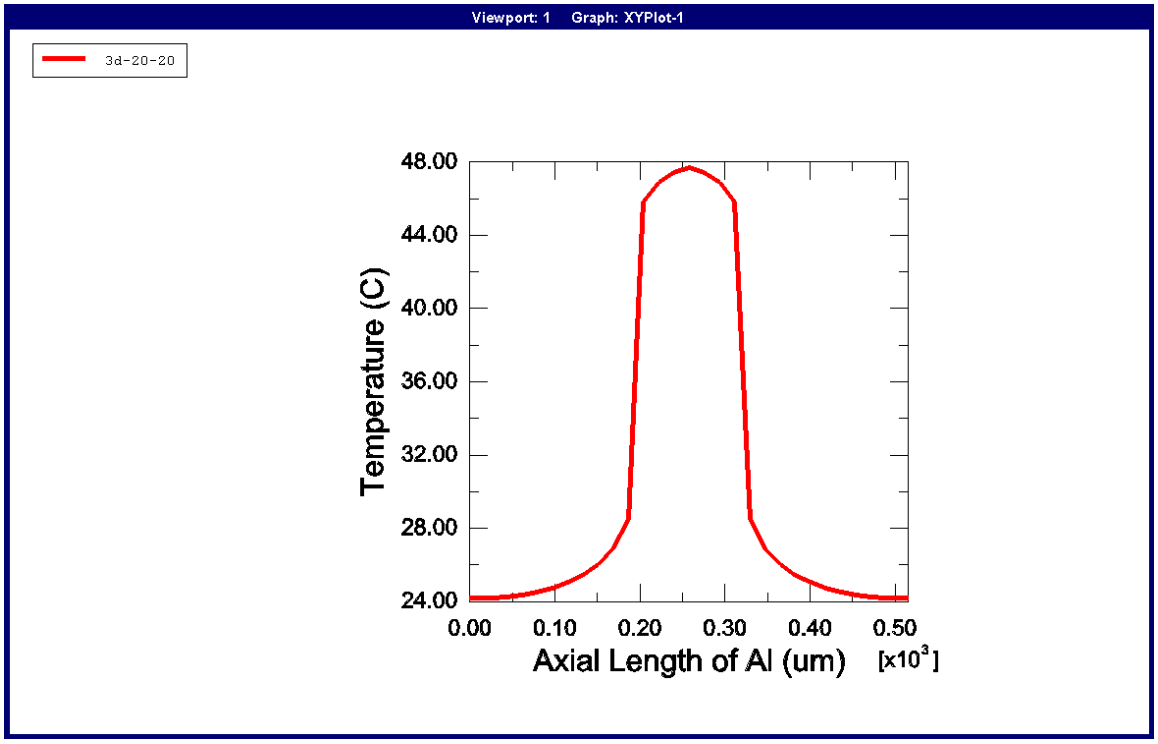


Fig. 23-2 XY plot of axial temperature distribution in Al (case 2)

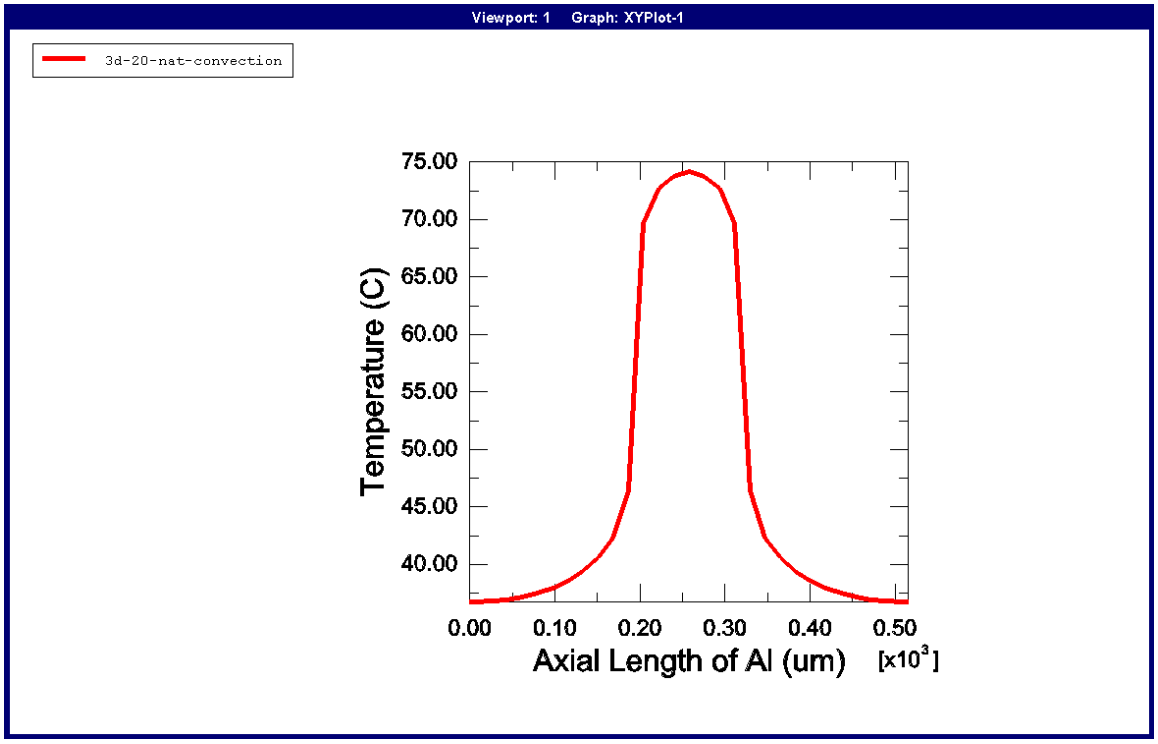


Fig. 24-2 XY plot of axial temperature distribution in Al (case 3)